Intelligent Self-adjusting Protection Algorithm for Smart LVDC Distribution Networks

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***Abstract*—With the increasing penetration of renewables, low voltage (LV) distribution networks face rising demands to accommodate an increasing range of renewable energies. Low voltage direct current (LVDC) distribution networks are considered as a viable approach to alleviate the strain on existing distribution networks. Nonetheless, establishing reliable and selective protection solutions is recognized as crucial challenges to facilitate the wide adoption of LVDC. Several existing protection algorithms focus on significant fault currents, fixed threshold settings, and high sampling frequency to establish effective coordination. However, these approaches are either constrained in low fault current scenarios or require expensive data acquisition techniques. To address such issues, this paper develops a novel self-adjusting based protection scheme. The method only utilizes the inherent post-transient voltage derivative (PTVD) sign and value with a self-adjusting mechanism to distinguish faults. The proposed method overcomes the selectivity limitations of existing voltage-based solutions when a lower sampling frequency is employed. The effectiveness is validated on an LVDC test network constructed in PSCAD/EMTDC and an RT-Box-based hardware test bed. Results under injected noise signals further demonstrate the robustness of the proposed method.**

***Index Terms*—LVDC, fault protection, smart transformer, post-transient voltage derivative, self-adjusting.**

I. Introduction

The shift towards low voltage direct current (LVDC) networks is mainly driven by the growing strain on existing LV networks, advancements in power electronics, the increasing prevalence of LVDC-based devices, and the demonstrated benefits of LVDC adoption [1]. Existing low voltage (LV) distribution networks are already facing challenges in accommodating the increasing presence of low carbon technologies, including heat pumps, micro wind, and solar generation. With the promotion of the net-zero concept throughout the world, especially in China, targets have been set to reach a carbon peak before year 2030 and carbon neutral by 2060 [2]. A high penetration of renewables and low carbon technologies is an effective means of facilitating carbon reduction. However, their integration poses significant challenges for existing LV networks in accommodating the growing electricity demand.

The adoption of smart LVDC distribution, particularly the photovoltaics-energy storage-direct current-flexibility (PEDF) system, has been widely recognized by industrial and research communities as a promising solution. This approach aims to alleviate pressure on existing LV networks, enhance their hosting capacity, and support the development of new infrastructure to meet the growing electricity demand from transportation and heating [2]. Numerous trials conducted worldwide, including in Finland, Germany, and China, have demonstrated significant benefits such as energy savings, improved controllability, and enhanced flexibility [3]. A key challenge identified by both research and industrial groups is the need for reliable, cost-effective DC protection solutions that ensure robust operation and high level of fault discrimination [4].

Advanced solid-state transformers (SSTs) have emerged as potential alternatives to traditional transformers in the transition from medium voltage (MV) to LV systems [5]. SSTs bring additional capabilities and controllability, and can provide both LVAC and LVDC supplies. From a protection perspective, SSTs typically produce lower fault currents than traditional transformers, potentially allowing the use of lower rating equipment [6]. However, the reduced fault currents may compromise the coordination of existing overcurrent protection solutions [7]. Moreover, employing overcurrent protection for its isolate may lead to unnecessary power outages.

In terms of the protection mechanisms, the DC fault transient current derivative (TCD) is highly sensitive to

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fault resistance following a transient, which may lead to maloperation when distinguishing between a nearby solid fault and a remote high-resistance feeder fault. Therefore, highly reliable and selective protection solutions are required. Numerous methods have been proposed that use transient voltage derivatives (TVD) as an alternative for DC fault detection, especially in HVDC and microgrid applications [8]. Nevertheless, these transient voltage behaviors are very sensitive to fault resistance when the sampling frequency is insufficient [9]. However, high sampling frequency devices increase cost in large-scale LVDC distribution networks, while lower sampling frequencies complicate protection threshold settings and may lead to coordination failures [10].

To address the challenges, this paper introduces an innovative self-adjusting post-transient voltage derivative (PTVD)-based protection scheme. In contrast to existing voltage and current based protection methods, the proposed scheme relies solely on PTVD characteristics following a transient voltage drop, rather than on the transient voltage drop and its surge derivatives. Additionally, the relays operate based on local DC voltage measurements using a self-adjusting mechanism, instead of fixed protection thresholds.

The rest of the paper is organized as follows. Section II outlines the primary challenges and constraints associated with existing LVDC protection solutions. Section III describes the principles underlying the self-adjusting PTVD-based protection mechanism, while Section IV presents simulation and hardware-based validations. Finally, Section V provides the conclusions drawn from the study.

II. LVDC Protection Challenges and Limitations of Existing Protection Solutions

A. Protection Challenges in SST Based LVDC Systems

The introduction of SSTs brings unique characteristics in DC faults that can influence current protection solutions. For instance, the active fault management capability of SSTs alleviates thermal stress on diodes, allowing the utilization of lower rating converters to ride through fault current endurance. However, this capability also extends the time required for overcurrent protection to distinguish faults in typical LVDC networks interfaced by two-level VSCs, thereby influencing protection selectivity [11].

The challenges in protecting SST-interfaced LVDC distribution networks extend beyond lower fault currents to include coordination among protection relays. For example, SSTs provide both AC and DC power outputs. In existing LVDC distribution networks, the fault current contribution from the main converter can be interrupted using overcurrent protection, without considering network interactions. In contrast, in SST-interfaced LVDC systems, blocking the SST may cause unnecessary power outages on both LVAC and MVDC sides.

Presently, LVDC protection mechanisms are primarily focused on two-level VSC-based LVDC distribution networks [12]. The development of protection algorithms for SSTs is still in the early stages due to the perceived simplicity of widely used two-level VSCs. Nonetheless, the increasing adoption of SSTs creates a demand for protection solutions with higher selectivity and reliability. Given the limited fault current contribution of SSTs compared with two-level VSCs, voltage-based protection solutions are considered a viable alternative for SST-interfaced LVDC systems.

B. Limitations of Existing Protection Algorithms

Studies in [9], [13], and [14] advocate for leveraging transient voltage characteristics for the protection of HVDC systems. For LVDC protection, a method based on current derivatives is proposed in [15], while the research outlined in [16] employs the current profile and communication links between line segment ends for faults discrimination. Furthermore, a novel protection technique utilizing transient functions for DC fault detection is introduced in [17], and an improved communication-based protection method is suggested in [18].

Advanced TVD-based solutions in HVDC applications primarily target MMC-based systems and rely on DC reactors, which are typically large due to their primary role in limiting fault currents [19]. However, large inductors at each LVDC feeder can lead to significant power loss and potentially impact system stability (e.g., 100 mH) [20]. On the other hand, MMCs are not typically used in LVDC systems due to their complexity and high cost. Additionally, the DC terminal configuration of MMCs differs from that of SSTs, as MMCs incorporate arm inductors throughout the fault path. Consequently, voltage features and their associated protection methods developed for MMC-based applications are not applicable to SST-interfaced LVDC distribution networks.

Existing derivative-based protection algorithms may be effective in identifying LVDC faults when using high sampling frequencies. However, the high costs associated with high-frequency sampling devices pose challenges in LVDC distribution networks. Utilizing metrology devices with lower sampling frequencies can reduce costs but introduces challenges in setting protection thresholds and fault discrimination for protection devices [21], [22]. For instance, Fig. 1 illustrates voltage derivatives with varying sampling frequencies for a fault located at the remote end. As seen, when the sampling frequency is reduced to 10 kHz, the transient voltage derivative for a fault located near the protection boundary falls below the fixed protection threshold for a fault resistance exceeding 0.23 Ω. This can lead to protection blinding and loss of protection coordination, highlighting the need for enhanced protection mechanisms tailored to LVDC distribution networks.

This issue can occur in derivative-based protection methods that compare surge derivatives of transient voltage drops against fixed protection thresholds, particularly

when the sampling frequency is low. To address these challenges, this paper proposes a novel self-adjusting PTVD-based protection scheme that relies solely on post-transient voltage behaviors following a transient voltage drop. The scheme employs self-adjusting thresholds, which are automatically adjusted by relays according to different fault scenarios.

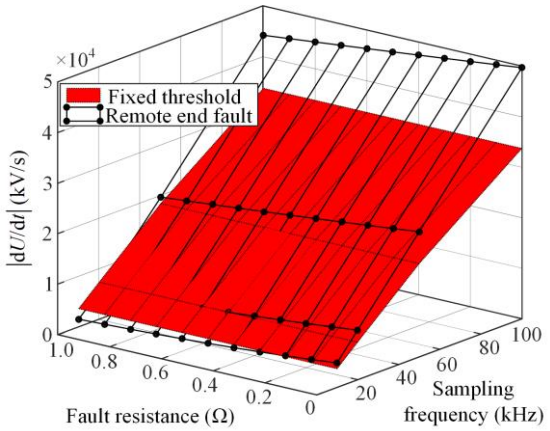

Fig. 1. Voltage derivatives with different sampling frequency.

III. Protecting SST Interfaced LVDC Distribution Networks Using Self-Adjusting PTVD Based Mechanism

This section introduces the mechanism of the proposed protection algorithm. A simplified circuit of SST-interfaced LVDC systems is depicted in Fig. 2. Since DC protection mainly focuses on the capacitor discharge stage, fault detection and coordination should be accomplished before the diode freewheeling stage. During the capacitor discharge stage, the converter can be simplified as a capacitor (C) with cable resistance (R) and inductance (L) in the fault path. The converter capacitor predominantly determines the system's capacitive behavior, since the cable capacitance (e.g., 12.1 nF/km [23]) is much smaller than the converter capacitance (e.g., 12 mF [24]). For simplicity, the cable is represented as an R-L series circuit, which can effectively reflect the cable's impact on LVDC transient responses [25], [26].

Each protection device includes a protection relay, a solid-state circuit breaker, and an assistive inductor. Taking the protection relay R_{a1} as an example, it operates if faults are located between relays R_{a1} and R_{a2} or on the upstream bus (i.e., Bus_1). Faults F1, F2, and F3 are defined as downstream faults of relay R_{a1}, while faults F4 and F5 are defined as upstream faults of relay R_{a1}, as depicted in Fig. 2. The following description is based on the protection relay R_{a1}. The diagram of the protection algorithm is illustrated in Fig. 3 and is described in details as follows.

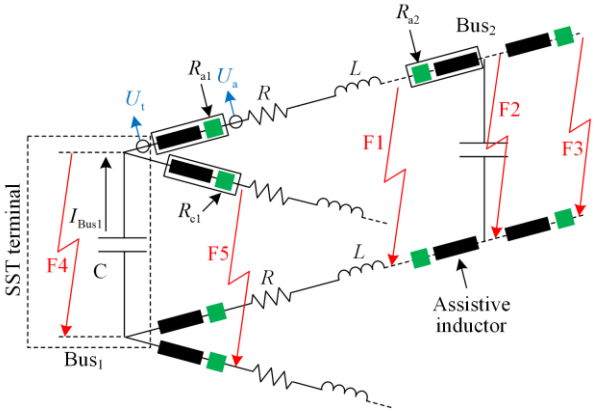

Fig. 2. A simplified circuit of SST-interfaced LVDC systems.

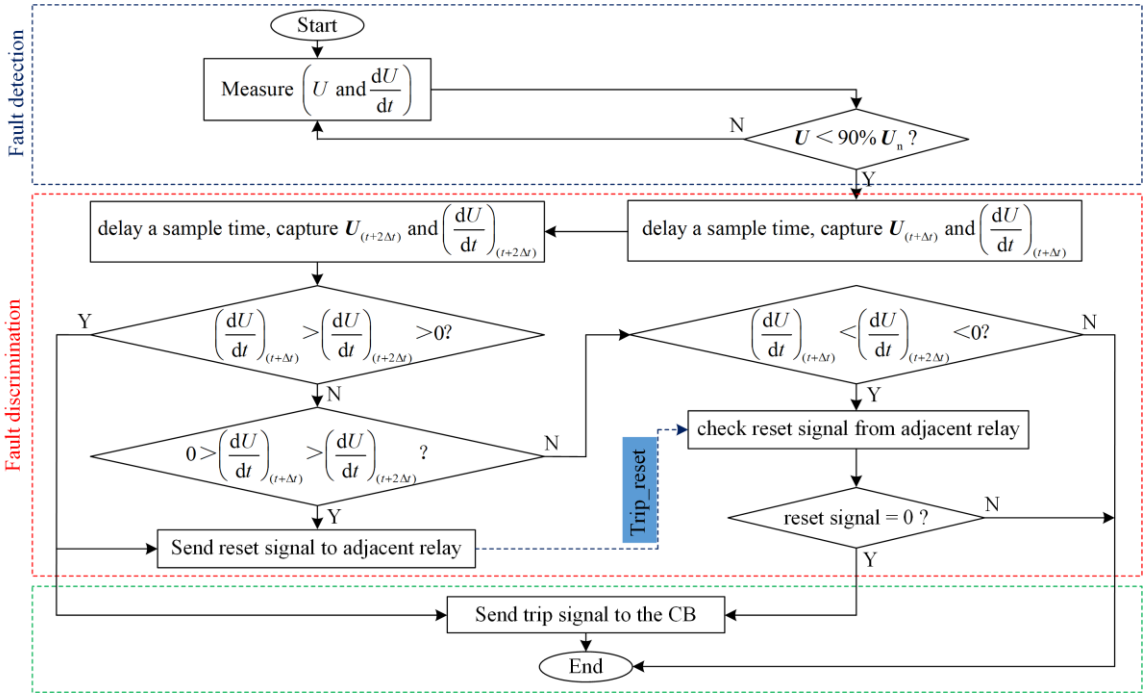

Fig. 3. Diagram of the self-adjusting PTVD-based algorithm.

A. Detection of LVDC Faults

The LVDC distribution network is considered to be under a fault condition if the voltage drops below 90% of the system nominal voltage (U_n), as depicted in Fig. 3. At present, no specific global regulations exist to govern DC voltage fluctuation in large-scale public LVDC distribution networks. Therefore, the threshold is selected based on the guidance from IEC60092-101, which primarily addresses DC distribution systems in marine application.

B. Protection Selectivity Based on Self-adjusting PTVD

1) Downstream Fault Discrimination

Under normal conditions, the voltage of relay R_{a1} (U_a) is the nominal voltage (U_n) and can be defined as:

$$U_t - U_a = L_a \times \frac{dI}{dt} \tag{1}$$

where U_t is the SST terminal voltage before relay R_{a1}; U_a is the voltage after relay R_{a1}; L_a is the assistive inductor of relay R_{a1}; and I is the current flowing through relay R_{a1}. Based on the LVDC fault characteristics [27], SST terminal voltage and current derivatives can be expressed respectively as:

$$U_t = \frac{U_0}{LC(s_1 - s_2)} \times \left(\frac{e^{s_2 t}}{s_2} - \frac{e^{s_1 t}}{s_1} \right) \tag{2}$$

$$\frac{dI}{dt} = \frac{U_0}{L \times (s_1 - s_2)} \times \left(s_1 e^{s_1 t} - s_2 e^{s_2 t} \right) \tag{3}$$

where U_0 is the initial voltage across the SST capacitor, definitions of $s_{1,2}$, α and ω_0 are expressed in (4) using resistance R, inductance L, and capacitance C in the fault circuit. Substituting (2) and (3) into (1) yields the voltage of R_{a1} as shown in (5). Substituting $t = 0$ and (4) into (5), the transient voltage of R_{a1} can be derived as (6).

$$\begin{cases} s_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega_0^2} \\ \alpha = \dfrac{R}{2L} \\ \omega_0 = \dfrac{1}{\sqrt{LC}} \end{cases} \tag{4}$$

$$U_a = U_t - L_a \times \frac{dI}{dt} = \frac{U_t}{LC(s_1 - s_2)} \times \left(\frac{e^{s_2 t}}{s_2} - \frac{e^{s_1 t}}{s_1} \right) - \frac{U_t L_a}{L \times (s_1 - s_2)} \times \left(s_1 e^{s_1 t} - s_2 e^{s_2 t} \right) \tag{5}$$

$$U_a = U_0 \times \frac{L - L_a}{L}, \quad t = 0 \tag{6}$$

Following a fault, the transient voltage of R_{a1} immediately drops to a value that is related to the nominal voltage, the ratio of the assistive inductor, and the inductor of the fault path. In theory, the voltage derivative is infinite. However, by using relatively high-fidelity DC transducers, such as those operating at 200 kHz [13], the transient voltage can be captured with an accuracy close to that described in (6). However, the adoption of such high-resolution DC measurement solutions in large-scale LVDC distribution networks leads to high cost and large size [10]. However, although using lower sampling frequency transducers reduces costs, the actual transient information may be missed, leading to protection selectivity issues. For example, Fig. 4 shows the voltage at a 20 kHz sampling frequency within the simplified circuit in Fig. 2, which is much lower than the original sampling frequency used in voltage derivative-based methods [13]. It can be seen that for a remote end fault (F1) with 0.45 Ω fault resistance, the value of TVD (i.e., dU/dt (0.4 Ω) labelled in Fig. 4) is almost equal to the TVD dU/dt threshold, whereas a higher fault resistance (i.e., >0.45 Ω) may cause protection failure.

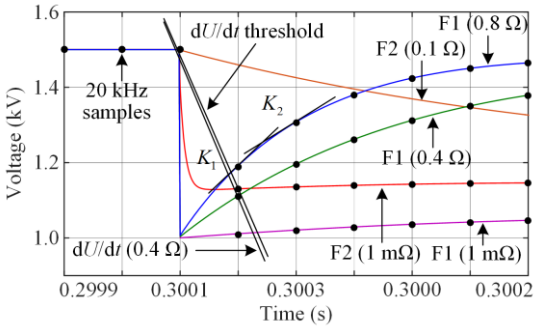

Fig. 4. Voltage and its derivatives with 20 kHz sampling frequency.

To address the issue, PTVD after a transient voltage drop offers a potential solution for effectively distinguishing resistive faults at lower sampling frequencies. Its mathematical properties can be derived as follows. Taking the derivation on both sides of (5), the PTVD of relay R_{a1} is expressed as (7), where the subscript "PT" denotes "post-transient". Setting $t = 0$ in (7), the PTVD of relay R_{a1} can be obtained in (8). After the transient voltage drop, the voltage of relay R_{a1} is positive, with its value determined by the nominal voltage, assistive inductance, and cable impedance within the fault path.

$$\left(\frac{dU_a}{dt} \right)_{PT} = \frac{U_t}{LC(s_1 - s_2)} \times \left(e^{s_2 t} - e^{s_1 t} \right) - \frac{U_t L_a}{L(s_1 - s_2)} \times \left(s_1^2 e^{s_1 t} - s_2^2 e^{s_2 t} \right) \tag{7}$$

$$\left(\frac{dU_a}{dt} \right)_{PT} = \frac{U_t L_a}{L^2} \times R, \quad t = 0 \tag{8}$$

The performance of the post-transient voltage described in Fig. 4 verifies that the PTVD magnitude increases with the increase of fault resistance, indicating a direct correlation between fault resistance and PTVD. This behavior contrasts with the conventional understanding of DC voltage fault characteristics, where the magnitude of the transient voltage derivative is expected to decrease and attenuate as the fault resistance increases. In addition, by differentiating both sides of (7), the secondary voltage derivative can be expressed in (9). By substituting (4) and *t=0* into (9), equation (10) is obtained, which is negative, indicating that the voltage derivative decreases after the fault occurs.

$$\left(\frac{\mathrm{d}^2U_{\mathrm{a}}}{\mathrm{d}t^2}\right)_{\mathrm{PT}} = \frac{U_{\mathrm{t}}}{LC(s_1-s_2)}\times\left(s_2\mathrm{e}^{s_2t}-s_1\mathrm{e}^{s_1t}\right)- \frac{U_{\mathrm{t}}L_{\mathrm{a}}}{L(s_1-s_2)}\times\left(s_1{}^3\mathrm{e}^{s_1t}-s_2{}^3\mathrm{e}^{s_2t}\right) \tag{9}$$

$$\left(\frac{\mathrm{d}^2U_{\mathrm{a}}}{\mathrm{d}t^2}\right)_{\mathrm{PT}} = -\frac{U_{\mathrm{t}}}{LC}-\frac{U_{\mathrm{t}}L_{\mathrm{a}}}{L}\left(s_1^2+s_1s_2+s_2^2\right),\ t=0 \tag{10}$$

Furthermore, to determine the boundary at which the voltage derivative begins to decrease, the time (e.g., t_1) to reach the maximum voltage is expressed in (11), obtained by setting (7) to 0. Also, by setting (9) to 0, the time (i.e., t_2) at which the voltage derivative changes sign is expressed in (12). Comparing (11) and (12), the time when the maximum voltage is reached is smaller than the time when the secondary voltage derivative changes sign. This indicates that PTVD decreases monotonically before reaching the maximum voltage after the fault transient.

$$t_1 = \frac{\ln\left(\frac{(Cs_2^2L_a+1)}{(Cs_1^2L_a+1)}\right)}{s_1-s_2} \tag{11}$$

$$t_2 = \frac{\ln\left(\frac{s_2(Cs_2^2L_a+1)}{s_1(Cs_1^2L_a+1)}\right)}{s_1-s_2} \tag{12}$$

This characteristic is demonstrated by the simulated voltage profiles shown in Fig. 4, where K_1 and K_2 represent the slopes of the F1 fault voltage profile. Since K_2 is smaller than K_1, the above mathematical derivation is validated. Based on this analysis and the voltage characteristics in Fig. 4, the relative profiles of downstream faults can be summarized in Table I.

TABLE I
PTVD FEATURES OF DOWNSTREAM FAULTS OF RELAY R_{a1}

Faults	sign	$\left\lvert\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{\mathrm{PT}}\right\rvert$
F1	+	decreasing
F2	–	decreasing
F3	–	increasing

Therefore, these characteristics can be used to distinguish downstream faults as illustrated in Fig. 3 and (13). After a fault is detected at time *t*, the relay delays sample time Δt and $2\Delta t$, and records PTVD $\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t+\Delta t)}$ and $\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t+2\Delta t)}$, where Δt depends on the sample time/sampling frequency. If the captured $\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t+\Delta t)}$ is bigger than $\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t+2\Delta t)}$, and both captured voltage derivatives exhibit positive signs, it indicates that the fault is in the downstream protected zone, shown as:

$$\text{downstream}:\left\{\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t+\Delta t)} > \left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t\ +\ 2\Delta t)} > 0 \right. \tag{13}$$

The value of $\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t+2\Delta t)}$ can be regarded as a protection threshold that dynamically self-adjusts through protection relays and sample times under different fault scenarios. This is based on the inherent LVDC PTVD features with an assistive inductor. In contrast to existing TVD-based methods, the proposed method eliminates the need for fixed thresholds to differentiate between different faults.

2) Upstream Fault Discrimination

When a resistive fault happens at the SST terminal (i.e., F4), the current flows from SST capacitor can be expressed as:

$$I_{\mathrm{Bus1}} = -C_{\mathrm{Bus1}}\times\frac{\mathrm{d}U_t}{\mathrm{d}t} \tag{14}$$

In this case, a resistor-capacitor (*R-C*) circuit is established, where I_{Bus1} is the current flowing out of SST capacitor, as shown in Fig. 2, C_{Bus1} is the SST capacitor, and U_t is the SST terminal voltage. The decreasing current of I_{Bus1} results in an increase in the voltage derivative of Bus_1, and the voltage of R_{a1} is similar to the terminal voltage. Under the F5 fault condition, when the upstream fault F5 happens, the current increases, and based on (14), voltage derivative of Bus_1 decreases. This feature can be used to discriminate upstream faults as presented in Fig. 3. The characteristics are summarized in Table II.

TABLE II
PTVD FEATURES OF UPSTREAM FAULTS OF RELAY R_{a1}

	sign	$\left\lvert\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{\mathrm{PT}}\right\rvert$
F4	–	decreasing
F5	–	increasing

Regarding the upstream fault protection mechanism, after the fault is detected at time *t*, the protection relay

captures PTVD $\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t+\Delta t)}$ and $\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t+2\Delta t)}$. If the captured $\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t+\Delta t)}$ is smaller than $\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t+2\Delta t)}$ with a negative sign, the fault is considered to be within the upstream protected region. Comparing the PTVDs of downstream and upstream faults, the PTVDs of relay $\mathrm{R_{a1}}$ under faults F2 and F4 are similar, both being negative with decreasing $\left|\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{\mathrm{PT}}\right|$. This may result in protection maloperation. To address this issue, the Trip_Reset signal is introduced, generated from the adjacent relays connected to the same terminal (e.g., relay $\mathrm{R_{c1}}$ which is adjacent to relay $\mathrm{R_{a1}}$).

Under the fault F2 condition, the voltage characteristics of relay $\mathrm{R_{c1}}$ are similar to the terminal voltage U_{Bus1} behavior described in (2), since the impedance between $\mathrm{R_{c1}}$ and the terminal is relatively small. By taking the derivatives of both sides, equations (15) and (16) can be obtained. Once the fault is initiated ($t = 0$), the terminal voltage derivative is 0, and the relative secondary derivative of the terminal voltage is negative, indicating that the terminal voltage derivative decreases under the F2 fault condition. This information can be used to allow relay $\mathrm{R_{a1}}$ to distinguish between F2 fault and F4 fault.

$$\left(\frac{\mathrm{d}U_{\mathrm{t}}}{\mathrm{d}t}\right)_{\mathrm{PT}} = \frac{U_0}{LC(s_1 - s_2)} \times \left(\mathrm{e}^{s_2 t} - \mathrm{e}^{s_1 t}\right) \tag{15}$$

$$\left(\frac{\mathrm{d}^2 U_{\mathrm{t}}}{\mathrm{d}t^2}\right)_{\mathrm{PT}} = \frac{U_0}{LC(s_1 - s_2)} \times \left(s_2 \mathrm{e}^{s_1 t} - s_1 \mathrm{e}^{s_1 t}\right) \tag{16}$$

In addition, for high resistive faults located out of the upstream protected region (i.e., F5), relay $\mathrm{R_{a1}}$ detects similar voltage derivative behavior to the upstream terminal fault (i.e., F4), as illustrated in Fig. 5. As the fault resistances of F4 and F5 increase, their voltage characteristics become similar, which may lead to maloperation when the fault is identified outside the upstream protected region.

In this case, a trip reset signal is sent by the adjacent relay $\mathrm{R_{c1}}$ to relay $\mathrm{R_{a1}}$ to internally reset the trip signal, which is generated when the captured PTVD of relay $\mathrm{R_{c1}}$ is positive (regarding to fault F5 condition) or when the PTVD of relay $\mathrm{R_{c1}}$ decreases with a negative sign (with respect to the fault F2 condition). The formulas for upstream fault discrimination can be expressed in (17) and (18), where U_{ad} is the voltage signal captured by the adjacent relay, and the Trip_reset (TR) signal (only 0 or 1) is generated locally by the adjacent relays connected to the same terminal. Using the *Trip_reset* signal, relay $\mathrm{R_{a1}}$ can distinguish the upstream and downstream internal and external faults.

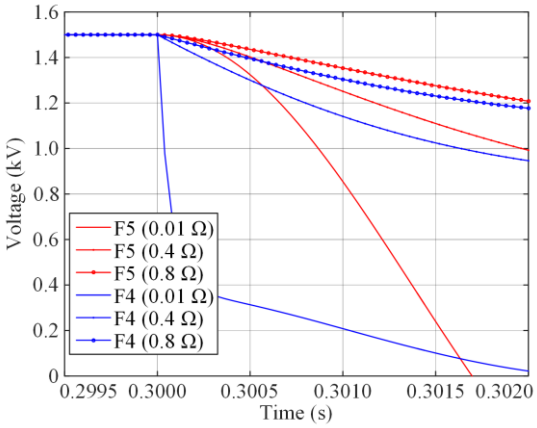

Fig. 5. Upstream faults (F4 and F5) of relay $\mathrm{R_{a1}}$.

In contrast to the existing TVD-based protection method, the proposed self-adjusting protection scheme relies exclusively on PTVD. This approach not only eliminates the need for threshold settings and current signals to indicate fault directions, but also demonstrates enhanced fault discrimination capabilities against both downstream and upstream resistive faults.

$$\text{upstream}: \begin{cases} \left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t+\Delta t)} < \left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t+2\Delta t)} < 0 \\ \mathrm{Trip\_Reset} = 0 \end{cases} \tag{17}$$

$$\mathrm{TR}: \begin{cases} 1, \text{ if } \left(\frac{\mathrm{d}U_{\mathrm{ad}}}{\mathrm{d}t} > 0\right) \left| \left(0 > \left(\frac{\mathrm{d}U_{\mathrm{ad}}}{\mathrm{d}t}\right)_{(t+\Delta t)} > \left(\frac{\mathrm{d}U_{\mathrm{ad}}}{\mathrm{d}t}\right)_{(t+2\Delta t)}\right)\right. \\ 0, \text{ if } \left(\left(\frac{\mathrm{d}U_{\mathrm{ad}}}{\mathrm{d}t}\right)_{(t+\Delta t)} < \left(\frac{\mathrm{d}U_{\mathrm{ad}}}{\mathrm{d}t}\right)_{(t+2\Delta t)} < 0\right) \end{cases} \tag{18}$$

3) SST Self-protection and Coordination Mechanism

On SST protection, the proposed protection algorithm can be integrated into SST to discriminate between faults at the SST terminal and those at the start of outgoing feeders. SST terminal voltage can be described in (2), and the protection scheme of (17) and (18) can be applied. After detecting a fault condition, the voltage derivatives are compared. If the captured $\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t+\Delta t)}$ is smaller than $\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t+2\Delta t)}$ and the sign is negative, the fault is identified to be at the main SST terminal; otherwise, it is located at downstream feeders. In addition, reset signals are received from the relays at the start of the outgoing feeders. Based on these two scenarios, the SST provides two main functionalities. For faults detected outside the SST terminal, it limits the

fault currents to ensure resilient and secure operation of downstream breakers. In addition, if the fault is identified in the main terminal, the SST interrupts the current feeding into the LVDC distribution networks.

IV. Validation of the PTVD Based Protection Method

The effectiveness of the proposed protection algorithm is validated via PSCAD/EMTDC simulation studies and hardware-in-the-loop (HIL) tests based on RT-Box. A detailed LVDC test network is built in PSCAD/EMTDC. The subsequent sections outline the test network model and simulation studies under various fault scenarios.

A. Modelling of the LVDC Test Network

The test network is modeled as illustrated in Fig. 6, which incorporates a two-stage SST to interface the LVDC system with an 11 kV AC grid. At the DC point of common coupling (PCC), the SST provides a pole-to-pole voltage of 1.5 kV. The AC input is simulated as a voltage source with a resistor-inductor (*R-L*) configuration. Cables are represented using an equivalent *R-L* circuit, and each feeder is 500 m in length. The relevant parameters are detailed in Table III.

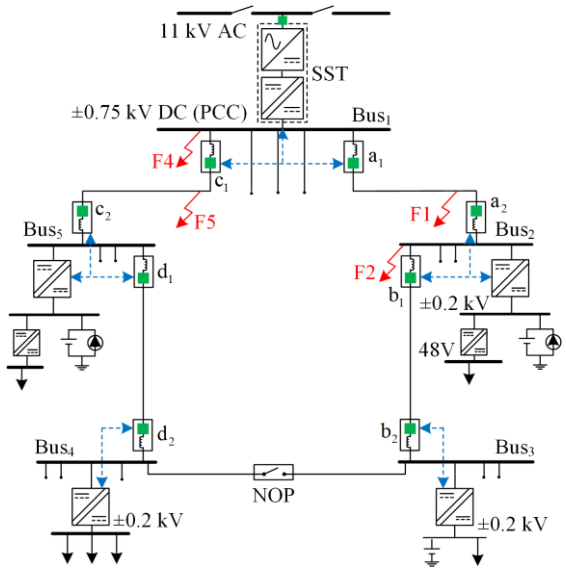

Fig. 6. A representative test distribution network.

TABLE III
LVDC Model Details [24]

Key item	Value
AC grid (kV)	11
Fault level (MVA)	156
SST rating (MVA)	1
MVDC supply (kV)	20
LVDC supply (kV)	1.5
Cables detail	0.164 Ω/km, 0.24 mH/km
customer rating (kW)	200
Assistive inductors (mH)	0.12

The SST's AC/DC VSC operates in V_{DC}-Q (20 kV – 0 kvar) control mode. During fault conditions, the SST employs a current-based phase-shift control to limit the steady-state fault current [28]. Based on the protection scheme, the converter can terminate the fault current by deactivating the power electronic switches.

B. Modelling of the PTVD based Protection Algorithm

The protection algorithm, illustrated in Fig. 3, is modeled as depicted in Fig. 7. The relays capture only local voltage measurements, which are utilized in fault detection, fault discrimination, and in generating trip signals for the relevant breakers and reset signals for upstream adjacent relays under fault conditions. Simplified DC circuit breakers, with a 0.5 ms isolation time, are modeled [29] to clear faults. To ensure the accuracy and reliability of the proposed protection scheme, an authentic noise signal is obtained from a laboratory DC current transducer and incorporated into the measured current signals during case studies. Research in [30] suggests that optimizing the sampling frequency and employing a low-pass filter are effective in mitigating the impact of noise on DC current and voltage signals. Consequently, a conventional moving average filter with a 1 ms window is applied in the PSCAD model. Additionally, a sampling frequency of 20 kHz is employed during the simulation studies to eliminate the noise impact, which is about 40 dB on voltage derivatives, as well as testing the effectiveness of the proposed scheme at a low sampling frequency. Furthermore, since relays are typically installed only a few meters apart on the same bus [31], the resulting communication delay is negligible, especially considering the protection system's 20 kHz sampling rate.

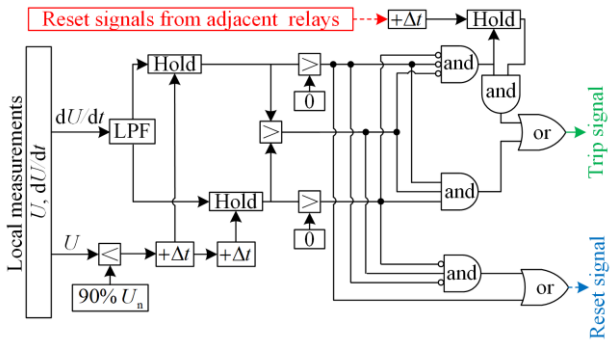

Fig. 7. Model of the PTVD based protection scheme.

C. Testing of the Proposed Protection Scheme

The following part validates the performance of the proposed self-adjusting PTVD-based protection scheme using downstream and upstream fault scenarios (i.e., F1, F2, F4, and F5) applied at 0.3 s.

1) Downstream Fault Discrimination Capabilities

When the F1 fault happens, relays R_{a1} and R_{a2} monitor the transient voltage drops as shown in Fig. 8.

When they fall below 90% of U_n, the fault is detected. Then, the held voltage derivatives are shown in Fig. 9, indicating the captured PTVD $\left(\frac{dU}{dt}\right)_{(t+\Delta t)}$ by relay R_{a1} is bigger than $\left(\frac{dU}{dt}\right)_{(t+2\Delta t)}$. Thus, the fault is identified as in its downstream protected zone as explained in (13), and trip signals are sent to the associated breakers. Relay R_{a2} locates the F1 fault and also generates a trip signal, so the fault current is interrupted as illustrated in Fig. 10. The F1 fault is cleared, and the PCC voltage is recovered to the nominal voltage within 2 ms as shown in Fig. 8.

Regarding the F2 fault, the captured PTVD $\left(\frac{dU}{dt}\right)_{(t+\Delta t)}$ by relay R_{a1} is smaller than $\left(\frac{dU}{dt}\right)_{(t+2\Delta t)}$, as shown in Fig. 11, which aligns with the feature presented in Table I. Meanwhile, a reset signal is generated by relay R_{c1}, whose captured $\left(\frac{dU}{dt}\right)_{(t+\Delta t)}$ is larger than $\left(\frac{dU}{dt}\right)_{(t+2\Delta t)}$ with a negative sign as illustrated in Fig. 12. That aligns with the profile presented in (15) and (16). With the implementation of the protection mechanism presented in (17) and (18), the F2 fault is recognized as an external fault by relay R_{a1}, and no trip signal is generated by relay R_{a1}. The performance of relay R_{a1} under the F1 and F2 fault conditions demonstrates the effectiveness of the proposed protection mechanism in distinguishing downstream faults.

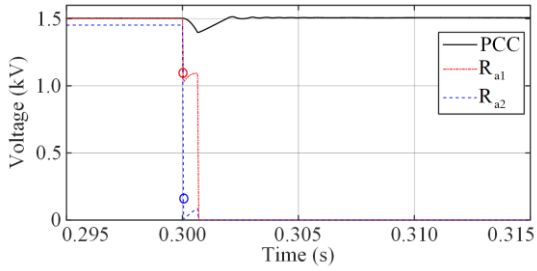

Fig. 8. Voltage of PCC, R_{a1}, and R_{a2} under F1 fault condition.

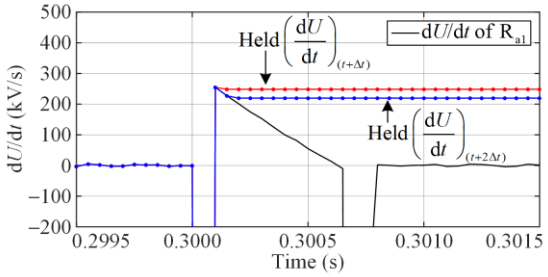

Fig. 9. PTVD of R_{a1} under F1 fault condition.

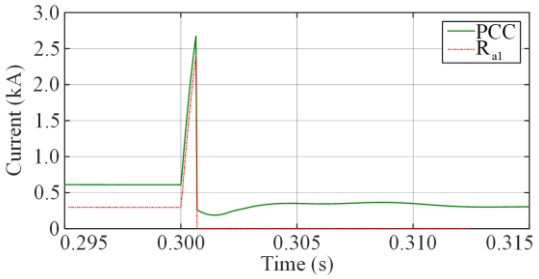

Fig. 10. Current of PCC and relay R_{a1}.

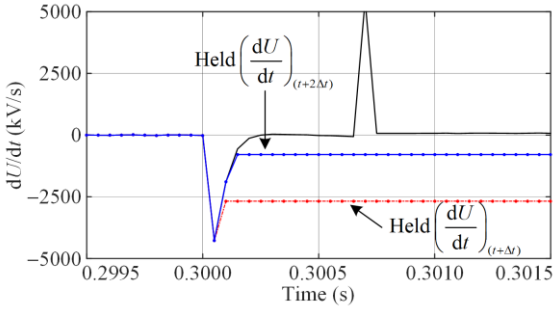

Fig. 11. PTVD of R_{a1} under F2 fault condition.

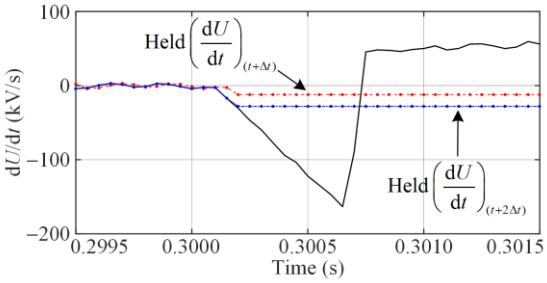

Fig. 12. PTVD of R_{c1} under F2 fault condition.

2) Upstream Fault Discrimination Capabilities

For the upstream fault scenarios, F4 and F5 faults with 0.01 Ω are applied. Once the F4 fault occurs at 0.3 s, relay R_{a1} detects the fault condition once the voltage drops below 90% of its nominal value, with the captured PTVD $\left(\frac{dU}{dt}\right)_{(t+\Delta t)}$ being smaller than $\left(\frac{dU}{dt}\right)_{(t+2\Delta t)}$ and carrying a negative sign, as shown in Fig. 13. Relay R_{c1} exhibits a similar voltage profile, and therefore, it does not issue a reset signal to relay R_{a1}. Consequently, relay R_{a1} sends a trip signal to its connected circuit breaker. Since the fault is located at the main busbar, the SST's DAB converter blocks itself to stop feeding grid current to the LVDC distribution network, as shown in Fig. 14.

In the event of an upstream external fault, e.g., F5, relay R_{a1} detects the fault condition when the voltage drops below 90% of the nominal voltage. It monitors and compares PTVD at time $t+\Delta t$ to that at time

$t+2\Delta t$, as depicted in Fig. 15, which exhibit a higher negative value than $\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t+2\Delta t)}$. Thus, relay R_{a1} recognizes that the fault F5 is outside the protected region, and no trip signal is generated.

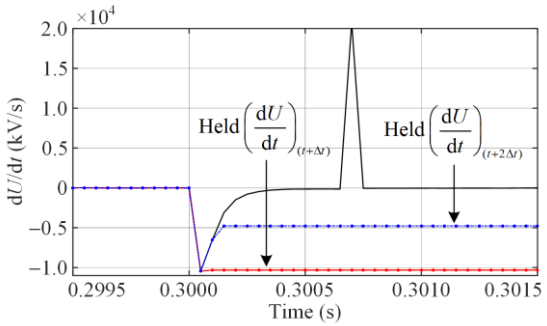

Fig. 13. PTVD of R_{a1} under F4 fault condition.

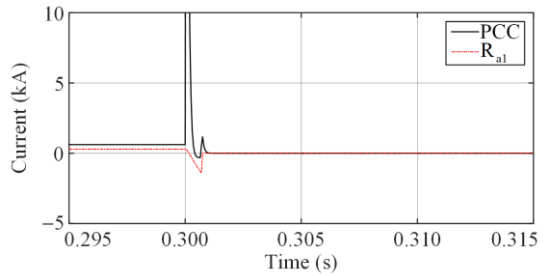

Fig. 14. Current of PCC and R_{a1} under F4 fault condition.

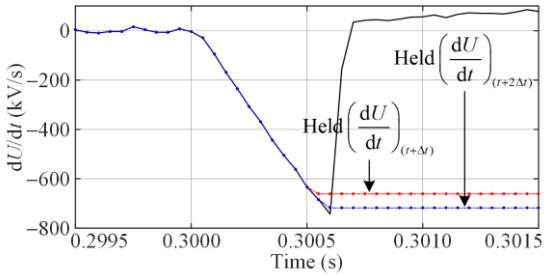

Fig. 15. PTVD of R_{a1} under F5 fault condition.

For relay R_{c1} under the F5 fault condition, the captured $\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t+\Delta t)}$ is larger than $\left(\frac{\mathrm{d}U}{\mathrm{d}t}\right)_{(t+2\Delta t)}$ with a positive sign as shown in Fig. 16. Therefore, fault F5 is located within its downstream protected region and is cleared by relays R_{c1} and R_{c2}, and the grid is subsequently recovered as shown Fig. 17.

Additionally, in the case of high resistive upstream external fault, relay R_{a1} may generate a trip signal, as demonstrated in Fig. 5. However, because the fault is first located within the protected region of relay R_{c1}, relay R_{c1} sends a reset signal within 0.1 ms to relay R_{a1} to prevent its maloperation.

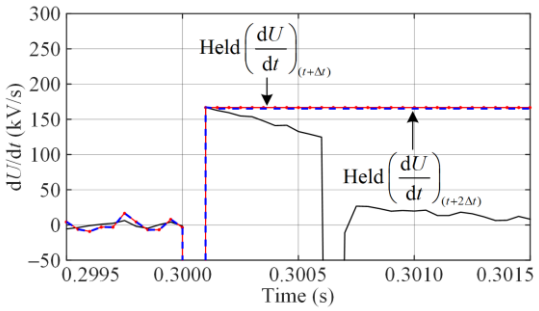

Fig. 16. PTVD of R_{c1} under F5 fault condition.

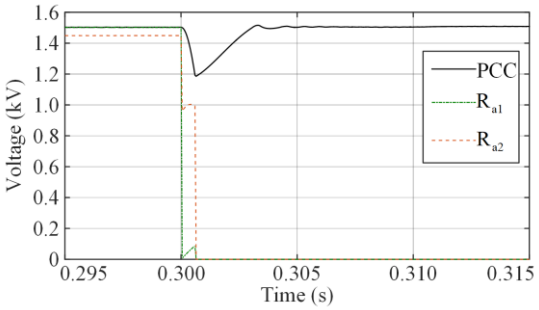

Fig. 17. Voltage of PCC, R_{c1}, and R_{c2} under F5 fault condition.

D. Resistive Fault Discrimination Capability

Regarding high-resistance fault discrimination capability, the proposed protection mechanism relies on the shape of PTVD rather than the transient voltage surge-induced derivatives, as shown in (17) and (18). PTVD with a self-adjusting threshold at various sampling frequencies is illustrated in Fig. 18.

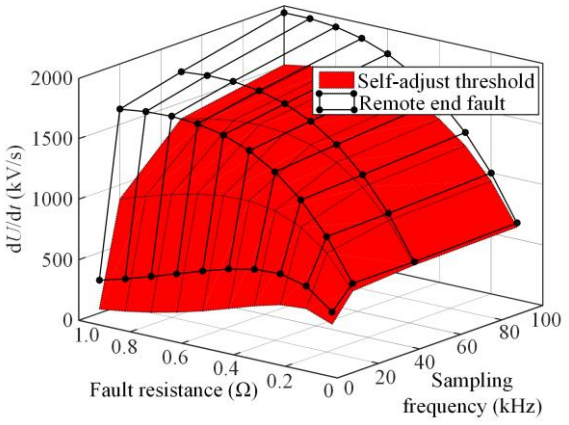

Fig. 18. Self-adjusting thresholds with sampling frequency.

With the assistive inductor in the circuit (i.e., 0.12 mH), the voltage derivatives during remote end faults consistently exceed the self-adjusting thresholds, thereby preventing any protection failures. Compared to the performance of the existing voltage derivative-based methods demonstrated in Fig. 1, the proposed technique can accommodate fault resistances ranging from solid to 1 Ω at a lower sampling frequency of 10 kHz when a 0.12 mH assistive inductor is employed. Increasing the

assistive inductor from 0.12 mH to 3 mH extends the protection boundary for fault discrimination, allowing the proposed method to tolerate fault resistances of up to 33 Ω, as illustrated in Fig. 19. This range is approximately four times larger than that of existing TVD-based methods.

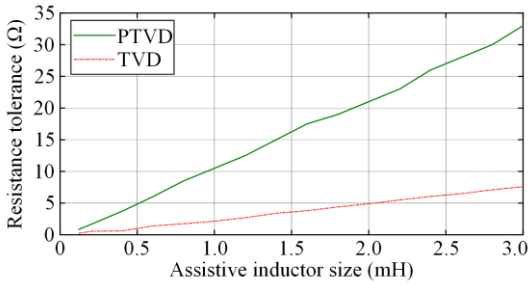

Fig. 19. Comparison of fault resistance tolerance.

E. Selectivity under Various Network Conditions

Regarding protection selectivity under varying network conditions, the analysis considers key factors such as grounding methods, network topologies, and cable lengths. The impact of these variables on the reliability and accuracy of the proposed protection scheme is thoroughly evaluated. Specifically, the interaction between grounding methods and fault current pathways is examined to ensure effective fault isolation. Variations in network topologies, such as radial and ring configurations, are considered to assess how the scheme adapts to complex system architectures. Additionally, differences in cable lengths are analyzed to determine their influence on fault behaviour and detection accuracy. This comprehensive discussion highlights the robustness of the proposed protection mechanism in maintaining selectivity across diverse operating scenarios.

1) Grounding Methods

There are several ground strategies available for DC systems, including ungrounded, unipolar solidly grounded, bipolar solidly grounded, and unipolar diode grounded configurations [32]. The simulation results presented in the above section primarily focus on pole-to-pole faults in an IT system where the neutral point is either ungrounded or grounded through a large resistance [33]. However, pole-to-ground faults in the IT system depend on its grounding point and have not been considered in the proposed method.

In this section, unipolar solidly grounded and bipolar solidly grounded strategies are discussed. For the unipolar solidly grounded strategy, the simplified circuit is shown in Fig. 20. Under pole-to-pole fault conditions, the pole-to-pole voltage U_a is similar to that in an ungrounded system shown in Fig. 8. However, the pole-to-ground voltage U_{ag} exhibits a higher transient voltage due to direct grounding of the negative pole, as shown in Fig. 21. Under pole-to-ground fault conditions in unipolar solidly grounded systems, U_a has a higher transient voltage as shown in Fig. 22, while U_{ag} exhibits a similar performance as presented in Fig. 8. Therefore, to ensure the effectiveness of the proposed protection scheme for unipolar solidly grounded systems, a combination of U_a and U_{ag} can be used.

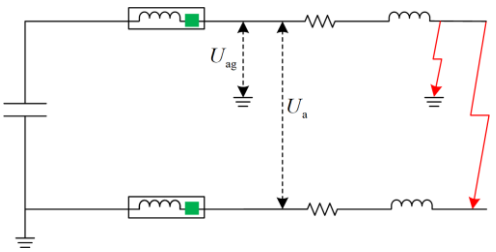

Fig. 20. A simplified circuits for a unipolar solidly grounded system.

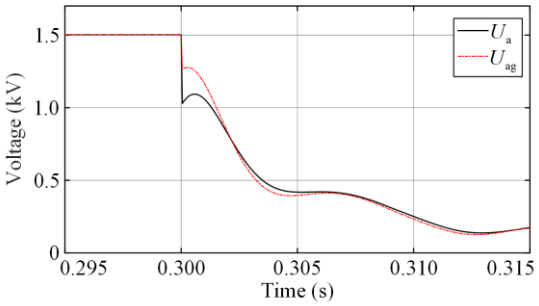

Fig. 21. U_a and U_{ag} voltage characteristics of Ra1 under F1 pole-to-pole fault in a unipolar solidly grounded system.

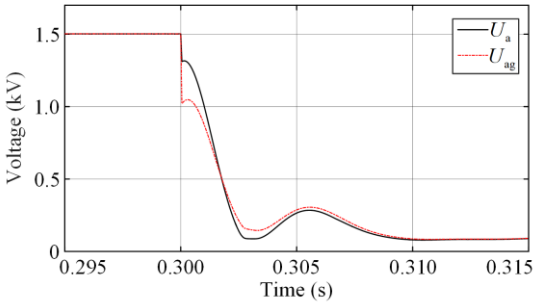

Fig. 22. U_a and U_{ag} voltage characteristics of R_{a1} under F1 pole-to-ground fault in a unipolar solidly grounded system.

For a bipolar solidly grounded system, a simplified circuit is shown in Fig. 23. The voltage characteristics of relay R_{a1} under F1 pole-to-pole and pole-to-ground faults in this configuration are illustrated in Figs. 24 and 25, respecively. It can be seen that the pole-to-pole voltage profile is similar to the voltage feature presented in Fig. 8.

However, for a pole-to-ground fault, due to the positive pole being short circuited to the middle grounding point, the post transient voltage of U_a is insignificant, while U_{ag} still provides distinct profile. Therefore, a combination of U_a and U_{ag} can be used to achieve

effective fault discrimination in a bipolar solidly grounded system. Furthermore, the effectiveness of this combined approach highlights the flexibility and adaptability of the proposed protection mechanism across different grounding strategies, ensuring consistent fault detection in complex DC networks.

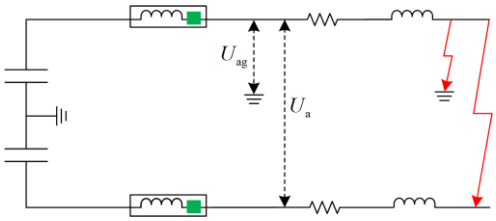

Fig. 23. A simplified circuit for a bipolar solidly grounded system.

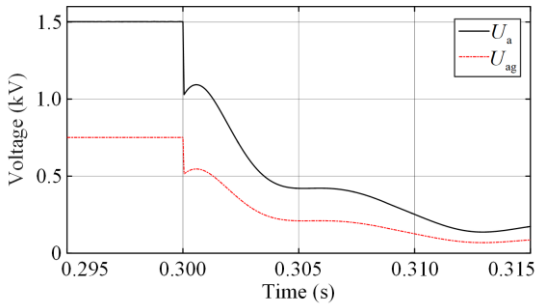

Fig. 24. U_a and U_{ag} voltage characteristics of R_{a1} under F1 pole-to-pole fault in a bipolar solidly grounded system.

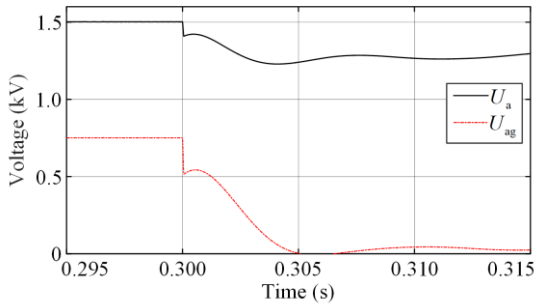

Fig. 25. U_a and U_{ag} voltage characteristics of Ra1 under F1 pole-to-ground fault in a bipolar solidly grounded system.

2) Configuration Topologies

Since the proposed protection method focuses on the post-transient stage, the impact of network configuration on fault discrimination is negligible. This is because the post-transient voltage characteristics presented in (8), which form the basis of the fault detection and discrimination process, remain consistent across different network configurations. To validate this, simulation results comparing the voltage characteristics of relay R_{a1} under F1 fault conditions in both ring and radial network configurations are presented in Fig. 26. As seen, the post transient voltage behaviors in radial and ring network configurations are similar, indicating that the proposed protection scheme reliably distinguishes faults regardless of the network topology, thereby demonstrating its robustness and adaptability to varying operational scenarios. This consistency highlights the scheme's effectiveness across applications, from simple radial networks to complex ring systems, without the need for additional adjustments or modifications to the protection algorithm.

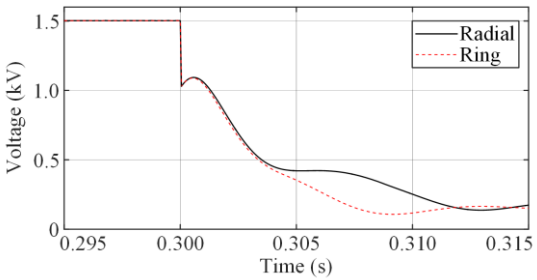

Fig. 26. Voltage characteristics of U_a for R_{a1} under an F1 pole-to-pole fault in radial and ring systems.

3) Cable Lengths

Regarding the impact of cable lengths, the post-transient voltage characteristics, as described in (8), are influenced by both the cable impedance and the assistive inductor. Variations in cable length affect the impedance of the circuit, leading to changes in the PTVD values, as illustrated in Fig. 27. Longer cables introduce higher resistance and inductance, which can alter the voltage response during fault conditions. However, the proposed protection scheme mitigates such variation by comparing PTVDs with different time delays, as formulated in (17) and (18). The results show that, despite variations in PTVD values due to different cable lengths, the underlying characteristics still adhere to the fault discrimination mechanism. This alignment ensures that the scheme can reliably distinguish between faults under different cable lengths.

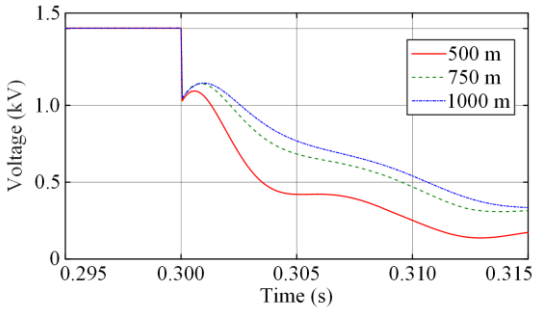

Fig. 27. Voltage characteristics of U_a for R_{a1} under an F1 pole-to-pole fault with different cable lengths.

Moreover, this robustness underscores the adaptability of the protection scheme to practical scenarios where cable lengths may vary due to different installation conditions or network expansion. By maintaining accurate and reliable fault discrimination even in the presence of significant variations in cable impedance, the proposed

method eliminates the need for recalibration or additional adjustments to the algorithm. This capability ensures high protection selectivity and simplifies implementation in both small-scale and large-scale DC networks, making the protection scheme highly practical and scalable for real-world LVDC distribution networks.

F. Validation in RT-box based Hardware Test Bed

The validation of the proposed self-adjusting protection method has been performed within an LVDC distribution network test bed with a relay control board represented in Fig. 28.

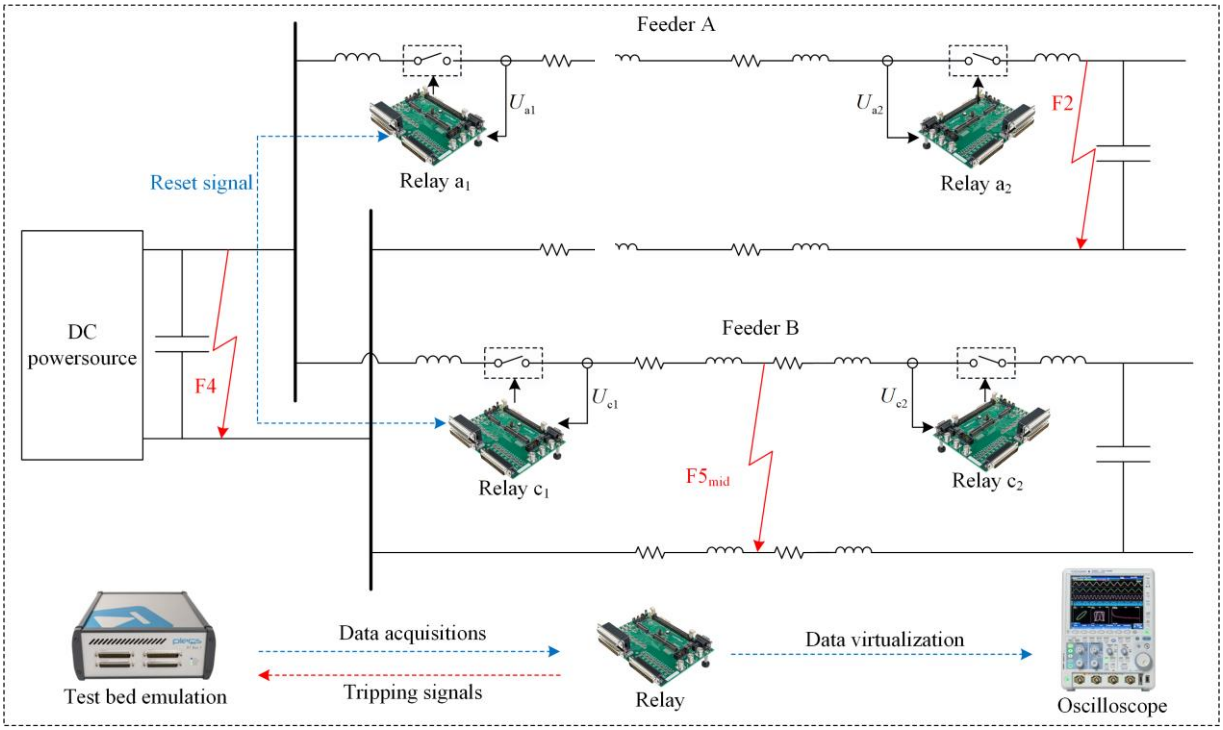

Fig. 28. Layout of hardware validation test bed.

This hardware configuration shown in Fig. 29 is designed to capture the main circuit data from the real-time simulation in RT-Box 1 which is used to emulate the circuit fault response. With the circuit running in RT-Box 1, the emphases are on data acquisition, implementation of protection algorithms, and signaling. The experimental setup initiates faults between the boundaries of the power converter interfaced capacitor and the related protection zones. Voltage measurements are taken at the boundaries of the protection zones to ensure accurate fault detection and discrimination. The main circuit runs in RT-box 1, and the analogue output is scaled within 3 V. The scheme is integrated in the TMS320F28335M-based control board with a 20 kHz sampling frequency and 12-bit analogue-to-digital converters.

The test circuit with the same parameter listed in Table III is modelled in PLECS and emulated in real-time using RT-box 1. In the experiments, three pole-to-pole faults with a fault resistance of 0.01 Ω are emulated by RT-Box 1, labeled as F2, F4, and $F5_{mid}$, representing faults located at the remote busbar, the PCC, and the upstream adjacent protected zone, respectively. The results of the fault contributions from the three faults are presented in Figs. 30–33.

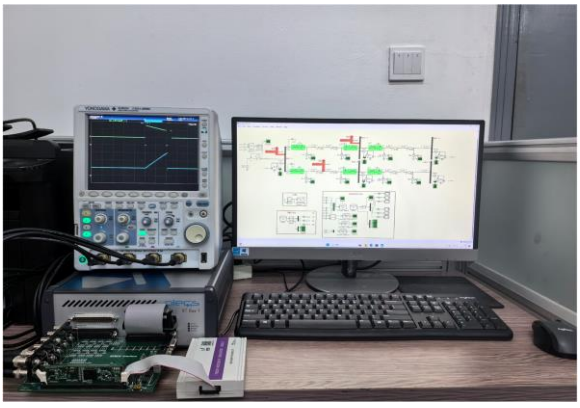

Fig. 29. Hardware test bed configuration.

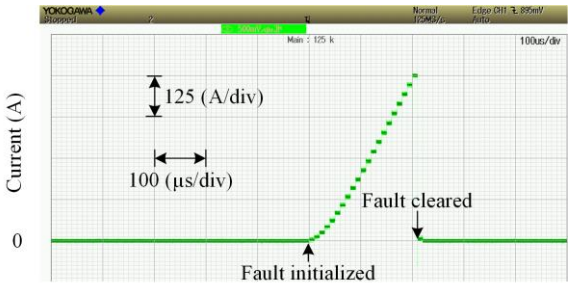

Fig. 30. Current of R_{a1} under F2 fault condition.

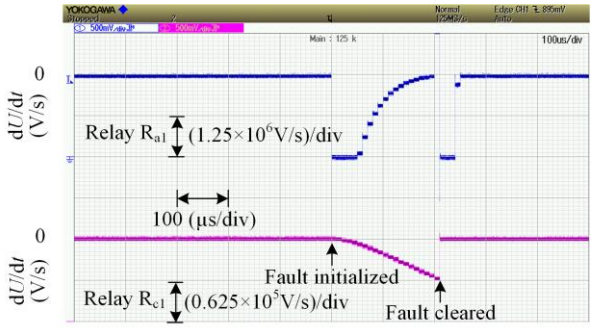

Fig. 31. PTVD of R_{a1} (upper) and R_{c1} (lower) under F2 fault condition.

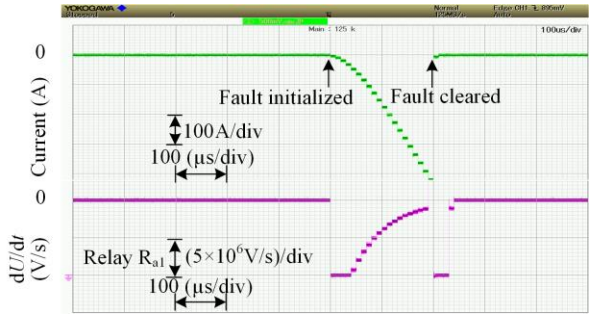

Fig. 32. Current and PTVD of R_{a1} under F4 fault condition.

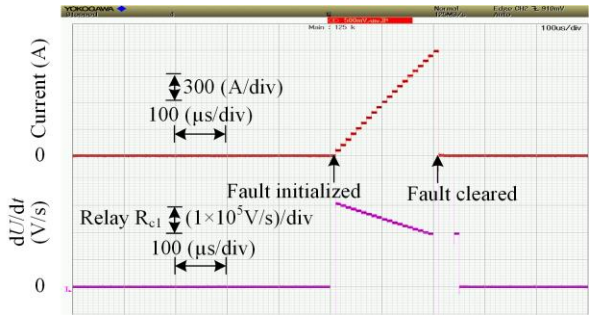

Fig. 33. Current and PTVD of R_{c1} under $F5_{mid}$ fault condition.

Under the F2 fault condition, fault current is interrupted within 200 μs by relay R_{a2}, as shown in Fig. 30. Meanwhile, the voltage derivative of relay R_{a1} is illustrated in the upper line of Fig. 31, showing an increasing trend with a negative sign. However, the voltage derivative of relay R_{c1} decreases with a negative sign as shown in the lower trace of Fig. 31. Based on (18), a reset signal is generated by relay R_{c1} and is sent to relay R_{a1}, ensuring no trip signal is generated by relay R_{a1}. Under the F4 fault condition, fault current is interrupted within 200 μs, as shown in the upper line in Fig. 32. In this case, PTVD of relay R_{a1} increases with a negative sign, as shown in the lower trace in Fig. 32. Relay R_{c1} exhibits similar behavior, and based on (18), no reset signal is generated. Thus, the fault is isolated by relays R_{a1} and R_{c1}. Regarding the $F5_{mid}$ fault, fault current is interrupted within 200 μs, as shown in the upper line in Fig. 33. PTVD of relay R_{c1} decreases with a positive sign, as illustrated in the lower line in Fig. 33. Based on (13), fault is cleared by relays R_{c1} and R_{c2}. The demonstrated reliable, fast and selective protection performance validates the effectiveness of the proposed protection scheme.

G. Comparison with Existing Derivative Based Methods

The comparison with existing methods, summarized in Table IV, highlights the enhanced performance of the proposed methods in several key aspects. Notably, it requires fewer metrology devices and smaller data set. Meanwhile, the proposed method demonstrates a stronger resistive-fault discrimination capability, even as the sampling frequency decreases from 20 kHz to 5 kHz with a 3 mH assistive inductor. The proposed scheme demonstrates an enhanced fault resistance tolerance, approximately four times greater than existing TVD-based methods and twice that of TCD-based methods, as illustrated in Fig. 19 and Table IV. Moreover, the proposed method only relies on PTVD measurement and eliminates the need for current information, thereby simplifying data acquisition while maintaining high reliability. This unique feature enhances its ability to discriminate resistive faults, even with reduced sampling frequency.

TABLE IV
COMPARISON WITH EXISTING DERIVATIVE BASED METHODS

		Proposed	[9]	[14]	[15]
Numbers of metrology devices		1– local U	2– local U– local I	2– Bus U– local U	1– local I
Required data set		U, PTVD, Trip_reset	U, dU/dt, I, dI/dt	U, dU/dt, K	I, dI/dt, d^2I/dt^2
Threshold setting		**No**	Yes	Yes	Yes
High resistive fault capability	5 kHz	**15 Ω**	3.5 Ω	3.5 Ω	7 Ω
	10 kHz	**33 Ω**	7.6 Ω	7.6 Ω	13 Ω
	20 kHz	**65 Ω**	15 Ω	15 Ω	20 Ω

V. CONCLUSION

This paper examines the distinctive characteristics of Post-Transient Voltage Derivative (PTVD) in LVDC distribution networks. Unlike Transient Voltage Derivative (TVD), PTVD does not diminish as fault resistance increases. Based on this feature, an intelligent self-adjusting PTVD-based protection scheme is presented for protecting DC bus and line faults in LVDC distribution networks. By incorporating PTVD with self-adjusting mechanism and PTVD-based reset signals, the proposed scheme can reliably detect and locate DC fault within 200 μs. This allows early-stage fault interruption, thereby reducing thermal stress on SSTs, improving post fault power quality, and enhancing the overall resilience of LVDC systems. Furthermore, employing the proposed self-adjusting PTVD-based protection scheme facilitates the identification and localization of high-resistance faults. It shows that DC faults

with a resistance up to 15 Ω can be precisely distinguished even with a reduced sampling frequency of 5 kHz. Such capability is approximately four times wider than that of existing voltage-based protection solutions in LVDC, highlighting the innovative and superior capabilities of the proposed method. In addition, simulation results confirm that the proposed method remains effective under signal noise levels up to 40 dB, demonstrating its noise immunity and robustness under practical operating conditions. This presents promising prospects for future applications in LVDC distribution networks.

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AUTHORS' CONTRIBUTIONS

Dong Wang: full-text writing, construction of the paper framework, software, and simulation. Pengfei Hu: methodology. Yu Cao: Hardware in the loop validation. Mazheruddin Syed: Supervision and proof reading. All authors read and approved the final manuscript.

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AVAILABILITY OF DATA AND MATERIALS

Not applicable.

DECLARATIONS

Competing interests: The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this article.

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