# Interharmonic Current Differential Protection Scheme for Converter-based Hybrid AC/DC Microgrids

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***Abstract*—The limitation of fault currents from converter based distributed generators (CBDGs) in hybrid AC/DC islanded microgrids poses a significant challenge for microgrid protection. This paper presents a novel interharmonic current differential protection scheme for the AC side of hybrid AC/DC islanded microgrids supplied by CBDGs. During faults, the proposed scheme exploits the varying interharmonic components of the currents at both terminals of the faulted line, arise due to variations in the droop-based no-load frequency limits of the interlinking converters (ICs) and the CBDGs. By leveraging these variations, the scheme effectively detects and isolates internal faults within the AC sub-grid, enhancing system reliability. The effectiveness of the suggested scheme is assessed using an enhanced IEEE33-bus hybrid AC/DC microgrid modelled in PSCAD/EMTDC, demonstrating its ability to reliably detect and isolate faults under various operating conditions. Additionally, the scheme is further evaluated using a real-time hardware-in-the-loop experimental setup implemented on an RTDS platform, validating its practical applicability. The simulation and experimental results validate that the presented protection scheme accurately discriminates between normal and faulty conditions across various fault locations, types, and resistance values. This discrimination is achieved without requiring high-bandwidth communication, overcoming a key limitation of existing protection schemes and improving feasibility in real-world deployments.**

***Index Terms*—Converter-based distributed generator (CBDG), differential protection scheme, hybrid AC/DC islanded microgrid, interlinking converter (IC).**

## I. Introduction

Hybrid AC/DC microgrids are gaining increased popularity for their enhanced efficiency, reliability, and stability in utilizing distributed generators (DGs) [1]. Despite careful design and operation in distribution cables and lines in hybrid microgrid, faults remain inevitable. The difference in fault current contributions from inverter-based and synchronous-based DGs adds further complexity to fault analysis and protection [2]. The situation is further complicated when considering the influence of a wide range of fault resistances. Hence, developing a precise protection algorithm is crucial to ensuring the reliable performance of hybrid AC/DC distribution systems [3], [4].

Converter-based distributed generators (CBDGs) play a crucial role in modern active distribution networks by facilitating the integration of renewable energy sources and enhancing networks' flexibility and efficiency [5]. Unlike synchronous generators, CBDGs rely on power electronics interfaces to regulate voltage and frequency, making them adaptable to varying load and generation conditions. However, their fault current contribution is inherently limited due to limited overcurrent capability of power electronics devices, thereby posing challenges for fault detection and isolation in hybrid AC/DC microgrids. Overcoming these limitations is crucial for ensuring the reliable and efficient operation of active distribution networks [6], [7].

Several protection strategies have been proposed in the literature for AC-islanded microgrids with CBDGs, which can be categorized into passive and active schemes. Passive protection schemes do not interfere with the DG interface control and mainly rely on the selected relay detection and fault isolation features. On the other hand, active protection schemes utilize the DG interface control to inject specific disturbances to facilitate relay detection and fault isolation. In [8]–[15], various passive protection schemes have been proposed

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to identify the faults within these microgrids. For instance, protection schemes are developed based on direct and quadrature measurements of bus voltage [8], a combination of under-voltage relays (UVRs) with directional functions [9], and current's travelling waves [10], [11]. Additionally, other passive schemes have been introduced using wavelet decomposition of the current components [12], [13] and the phase shift angle between positive sequence bus voltage and line current [14]. Furthermore, a communication-based differential protection algorithm is proposed which utilizes a data mining approach to identify specific features for fault detection and isolation [15]. However, the primary challenge in implementing these techniques is the selection of appropriate threshold settings and features to accurately distinguish between faulty and non-faulty conditions, considering different system abnormalities.

To address these challenges, various active protection schemes have been adopted in [16]–[21] to overcome the negative consequences of the current limiting capacity of the CBDGs. In these approaches, the CBDG controller creates certain independent and distinguishable conditions in the network when a fault occurs, while these conditions are utilized to provide fault identification and detection processes. These schemes involve various techniques, such as regulating the sequence components of the CBDGs' currents in the presence of asymmetrical faults [16], introducing off-nominal output frequency during fault conditions [17], and injecting 5th [18] and 3rd [19] harmonic current components. In addition, an impedance-modulated harmonic current injection mechanism is employed to inject a combination of three unique orders (3rd, 5th, and 7th) of current harmonics [20], and a soft current limiter is utilized to inject interharmonic current [21] from each CBDG. Furthermore, these active schemes have presented several relaying schemes, including differential frequency relays, harmonic directional overcurrent relays (HDOCR), and interharmonic differential relays to detect and identify the faulted line. However, there are some drawbacks in the aforementioned active protection schemes. For instance, additional fault detection schemes are required for each CBDG to start the injection process. Besides, the schemes relying on 3rd harmonics injection can be blocked by the delta connection of the power transformers, affecting the protection performance. Further, the harmonic currents resulting from nonlinear loads can adversely degrade the performance of these schemes.

DC microgrids are rapidly gaining popularity due to their ability to incorporate renewable energy sources and provide a more efficient power supply. Several schemes have been presented in the literature to address the protection of DC microgrids, including those based on unit protection [22]–[24], enhanced differential protection [25], [26], the rate of change of the current [27], [28], travelling wave-based [29] and distance protection [30]. In addition, some of the existing schemes rely on incorporating passive components and utilizing algorithms such as short-time Fourier transform (STFT) and discrete wavelet transform (DWT) to detect high resistance faults [31], [32]. In [33], a unified protection scheme is proposed which utilizes an impedance-based relaying for a hybrid microgrid. Although this scheme effectively discriminates internal faults and accurately estimates fault locations, its practicality and reliability are compromised by, e.g., not accounting for the interlinking converters (ICs) contribution during fault conditions. Besides, its applicability has not been tested for the islanded microgrids. Furthermore, the adoption of an iterative technique may have the potential to impede its performance due to convergence issues.

Therefore, the primary objective of this paper is to introduce a novel AC protection scheme by examining the interaction between the ICs and CBDGs. In contrast, the DC side of the hybrid microgrid can be protected by one of the existing algorithms described in [22]–[32].

This paper presents a novel interharmonic current differential protection scheme designed to detect and identify AC faulted lines in AC/DC islanded hybrid microgrids with CBDGs. The proposed algorithm exploits the frequency variation between the ICs and CBDGs in the AC sub-grid, which is attributed to different droop-based no-load frequencies during fault conditions. Based on different frequency current components at the bilateral of the faulted line, the interharmonic current differential protection scheme is employed to detect and identify the faults within the AC sub-grid. The scheme utilizes the detection and comparison of the differential interharmonic currents with a predetermined threshold value. When the differential interharmonic current exceeds the threshold, necessary trip actions are initiated to promptly isolate the faulted line. The effectiveness of the proposed scheme is evaluated through simulations on a modified IEEE33-bus hybrid AC/DC microgrid and a real-time hardware-in-the-loop (HIL) experiment setup. The proposed scheme offers the following key contributions.

1) Simplified protection design: Eliminates the need for individual fault detection mechanisms for each CBDG, reducing system complexity.

2) Comprehensive fault analysis: Incorporates IC contributions during fault conditions, ensuring robust protection for the entire microgrid.

3) Accurate fault detection: Focuses on interharmonic current amplitudes at line ends, avoiding the reliance on fault current direction and enabling precise fault identification.

4) High fault resistance handling: Accurately identifies and isolates all fault types, including symmetrical

and asymmetrical faults, with high fault resistance handling up to 100 Ω.

The structure of the paper is as follows. Section II investigates the system description and the simulation model of CBDGs and ICs. Section III is dedicated to the analysis of fault conditions in hybrid AC/DC microgrids, while Section IV outlines the proposed differential interharmonic protection scheme. Section V evaluates the effectiveness of the suggested protection scheme using a 4-bus Canadian urban hybrid microgrid and the IEEE33-bus islanded hybrid microgrid powered by CBDGs, and presents the findings and results. Section VI provides experimental validation using a HIL setup to confirm the practical applicability of the proposed scheme. Finally, the conclusion is provided in Section VII.

## II. System Description and Simulation

CBDGs are essential for integrating renewable energy resources into modern power systems. They operate under two primary states: normal operation and fault conditions. During normal operation, the droop-based control strategy regulates the active and reactive power output to maintain voltage and frequency stability in the microgrid. Under fault conditions, the current control loops limit the fault current contribution, which prioritizes the protection of power electronic devices over fault current magnitude. This limitation impacts traditional protection schemes, which rely on high fault currents for fault detection [34]. However, CBDGs exhibit unique characteristics such as interharmonic frequency variations during disturbances, which may be exploited for advanced protection schemes. The theoretical foundation for these characteristics is derived from the interaction between droop control mechanisms and network impedance, which influences the distribution of current and voltage harmonics during faults. The block diagrams of the CBDGs and IC are presented in Figs. 1–3. They are integrated into the hybrid distribution systems through voltage source converters (VSC), which have limited overcurrent capability and are vulnerable to high fault currents. Typically, the maximum current capacity of CBDGs during short circuits is limited to 1.2–1.5 times rated current to prevent system damage [3], [35]–[37]. Furthermore, the hybrid microgrid analyzed in this paper is solidly grounded.

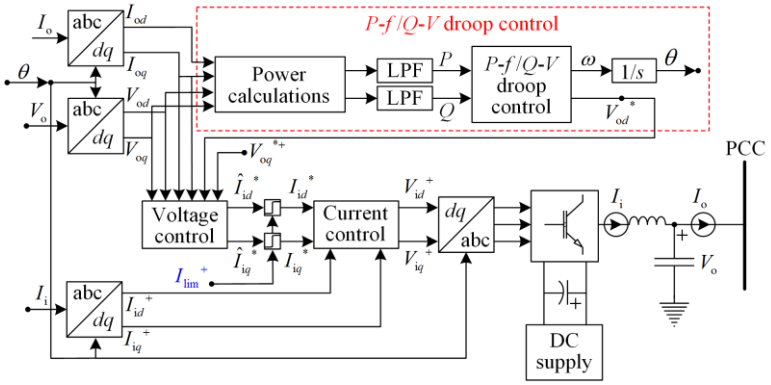



Fig. 1. Block diagram of the AC side CBDG control system including $P$-$f$/$Q$-$V$ droop control.

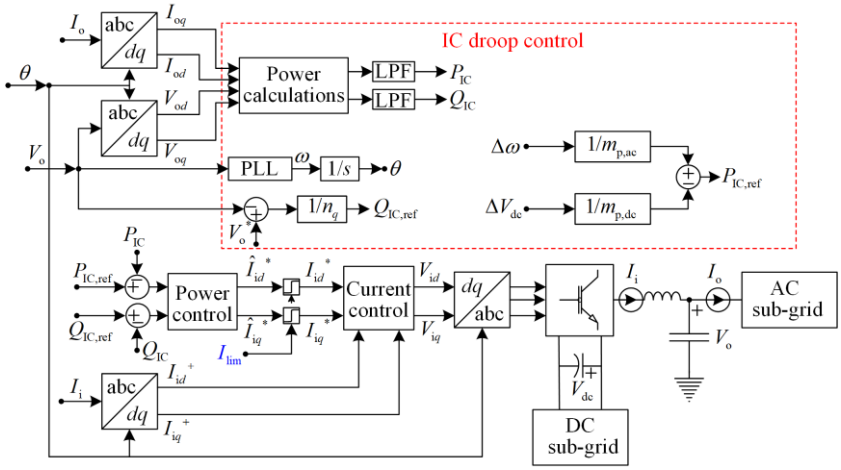



Fig. 2. Block diagram of the IC control system including $P$-$f$-$V_{dc}$ droop control.

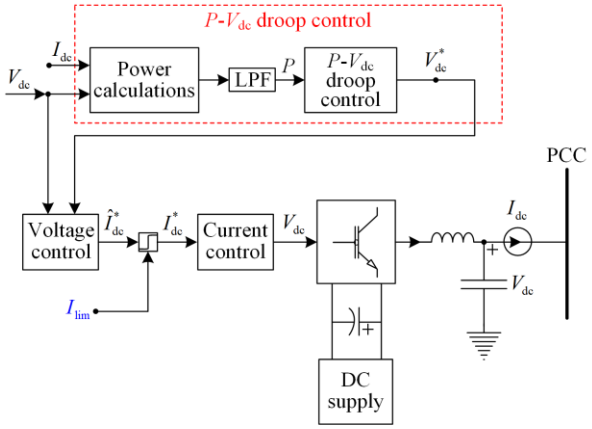



Fig. 3. Block diagram of the DC side CBDG control system including $P$-$V_{dc}$ droop control.

### *A. P-f/Q-V Droop Control of the AC CBDG*

The $P$-$f$/$Q$-$V$ droop control scheme is widely utilized and is essential for maintaining the stability of the AC CBDG in islanded microgrids. Besides, this approach ensures effective power sharing among the interconnected systems, providing optimal performance and system reliability [38]. This control scheme operates by regulating the voltage and frequency levels within the AC microgrid, with adjustments made in proportion to the reactive and active power generated by the distributed energy sources. Furthermore, it prevents voltage instability and frequency deviations that may lead to power disruptions. The droop equations are given as follows:

$$f_i = f^* - m_p \times P_{DGi} \tag{1}$$

$$V_{oi} = V_o^* - n_q \times Q_{DGi} \tag{2}$$

where $f_i$ and $V_{oi}$ are the amplitudes of DGs' reference frequency and voltage, respectively; $f^*$ and $V_o^*$ are the magnitudes of rated system frequency and no-load rated voltage, respectively; $P_{DGi}$ and $Q_{DGi}$ are the measured active and reactive power of the $i$th DG, respectively; $m_p$ and $n_q$ are the static droop factors and can be determined for a specific range of frequency and voltage, respectively, given as:

$$m_p = \frac{f_{max} - f_{min}}{P_{max}} \tag{3}$$

$$n_q = \frac{V_{max} - V_{min}}{Q_{max}} \tag{4}$$

where $f_{max}$, $f_{min}$, $V_{max}$, and $V_{min}$ represent the maximum and minimum frequency and output voltage values, respectively; $P_{max}$ and $Q_{max}$ represent the maximum active and reactive power that can be generated from the CBDG.

Figure 4 shows the droop curve that regulates DG's active power output in response to the frequency changes. It illustrates the correlation between frequency and active power, with a slope proportional to the droop constant $m_p$. The standard operating range of the CBDG frequency in islanded mode is $59\,\text{Hz} < f < 61\,\text{Hz}$ for system with nominal frequency of 60 Hz [38].

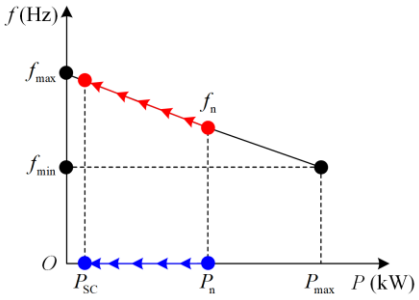



Fig. 4. $P$-$f$ droop characteristic curve of the AC CBDG.

### *B. P-f-V_dc / Q-V Droop Control for the IC*

The primary objective of the ICs is to establish a balance of power distribution between the DC and AC sub-grids, where the IC leverages two key loading indicators: frequency and voltage. The AC active power droop is frequency-dependent, which makes the frequency an ideal loading indicator for the AC side. Conversely, the DC active power droop is voltage-dependent, making the voltage the perfect loading indicator for the DC side. By monitoring and adjusting these indicators, the IC can effectively balance the active power distribution between the DC and AC sides, ensuring that neither sub-grid is overloaded nor underutilized.

As previously stated, active power sharing is linked to the changes in the AC side frequency, while the voltage changes pertain to the DC side of the hybrid microgrid. Consequently, effective active power sharing is achieved by ensuring that the frequency deviation ($\Delta f$) in the AC sub-grid is equivalent to the DC bus voltage deviation ($\Delta V_{dc}$) in the DC sub-grids [39]–[41]. However, since these parameters are measured in different units, normalization in per unit (p.u.) is required, as:

$$\Delta f = \frac{f_{IC}^* - f_i^{IC}}{0.5 \times (f_{max} - f_{min})} \tag{5}$$

$$\Delta V_{dc} = \frac{V_{dc}^* - V_{dc,i}}{0.5 \times (V_{dc,max} - V_{dc,min})} \tag{6}$$

where $f_i^{IC}$ and $f_{IC}^*$ represent the ICs' measured frequency and the reference frequency, respectively; $V_{dc,i}$ and $V_{dc}^*$ are the measured and reference DC voltage, respectively; the parameters $V_{dc,max}$ and $V_{dc,min}$ represent the maximum and minimum DC voltage values, respectively, which are utilized in the droop control of the ICs. Normalizing the measurements allows droop con-

trol implementation within the IC to guarantee active power sharing between the AC and DC sides.

Equations (5) and (6) generate inputs for the proportional controller by estimating the disparity between the measured and the reference frequency, as well as the DC voltage, respectively. The gain parameters for the frequency and voltage deviations are $1/m_{\mathrm{p,ac}}$ and $1/m_{\mathrm{p,dc}}$, respectively. The proportional controller's output is the difference in these control outputs, which determines the IC's active power reference, $P_{\mathrm{IC}}$, as defined in (7). The sign of $P_{\mathrm{IC}}$ relies on the direction of power flow and positive power injection is considered when power flows from the DC to the AC side, and vice versa, as illustrated in Fig. 5.

$$P_{\mathrm{IC}} = \Delta f \times 1/m_{\mathrm{p,ac}} - \Delta V_{\mathrm{dc}} \times 1/m_{\mathrm{p,dc}} \tag{7}$$

$$m_{\mathrm{p,ac}} = \frac{f_{\max} - f_{\min}}{P_{\max} + P_{\min}} \tag{8}$$

$$m_{\mathrm{p,dc}} = \frac{V_{\mathrm{dc,max}} - V_{\mathrm{dc,min}}}{P_{\max} + P_{\min}} \tag{9}$$

where $P_{\max}$ and $P_{\min}$ represent the maximum and minimum active power that can be transferred through the IC. The $P$-$f$-$V_{\mathrm{dc}}$ droop control characteristics, shown in Fig. 5, are designed for the IC based on the relationship between active power, AC frequency, and DC voltage. These characteristics regulate the IC's active power output and ensure appropriate power sharing between the DC and AC sides by adjusting the DC voltage and frequency. This paper presents IC droop control characteristics derived from frequency and DC voltage limits, determined by the ratings and permissible deviations in each sub-grid. The standard operating range for the system frequency is $59\ \mathrm{Hz} < f < 61\ \mathrm{Hz}$, and $0.95\ \mathrm{p.u.} < V_{\mathrm{dc}} < 1.05\ \mathrm{p.u.}$ for the DC voltage. To avoid overloading, the DC sub-grid's power injection through the IC is limited to $P_{\max}$. Importantly, the designed droop characteristics ensure the safe and reliable operation of the microgrid under various operating conditions [40].

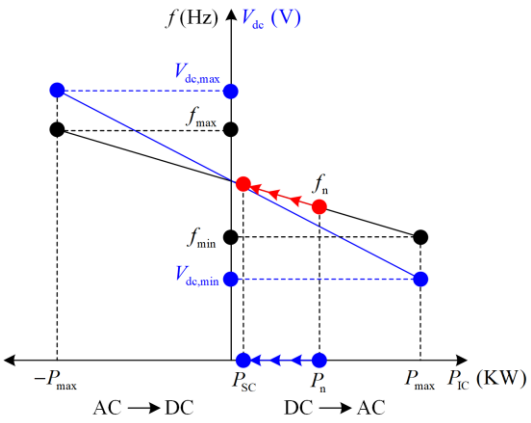



Fig. 5. $P$-$f$-$V_{\mathrm{dc}}$ droop characteristic curves of the IC.

## III. Analysis of Fault Conditions in Hybrid AC/DC Microgrids

This section explores the dynamics of faults in the AC side of hybrid AC/DC microgrids, focusing on bolted faults and high impedance faults (HIFs) in AC sub-grids. The investigation examines the effects of these faults on the generation of interharmonic currents and their impact on the output of CBDGs and ICs, particularly in terms of system frequency. This section provides a deeper understanding of fault behavior by analyzing fault formation, propagation, and their impact on microgrid components. This analysis is crucial for developing advanced fault detection and isolation mechanisms, which are essential for the reliability and safety of hybrid microgrids.

### *A. Impact of Bolted Faults on AC Sub-grid*

During bolted fault conditions, the creation of a low-impedance path at the fault location leads to a substantial voltage drop at the output terminals of the CBDGs and ICs. This sharp reduction in voltage allows fault currents to flow, which is subsequently limited by the current-limiting controls in the CBDGs and ICs. As a result, the active power generation from the CBDGs and ICs decreases significantly, depending on the fault severity and network impedance. Additionally, the voltage collapse at the faulted bus propagates through the system, disrupting power flow and potentially causing transient disturbances in connected components. These dynamics emphasize the need for robust protection schemes to detect and isolate such faults effectively, particularly in systems relying on CBDGs [34], [42].

Figure 6 illustrates a simple hybrid AC/DC microgrid system layout, featuring two CBDGs, an IC, and various loads connected to the AC side. Detailed specifications of the CBDGs, IC, and line parameters are included in Fig. 6. In a bolted fault scenario at F2, the active power output of the CBDG significantly diminishes, leading to an increase in the CBDG's frequency towards its maximum limit $f_{\max}$, which is typically 61 Hz within the selected operating frequency range, as demonstrated in Fig. 4. Concurrently, the decrease in active power from the IC prompts its frequency to average out at $(f_{\max} + f_{\min})/2$, typically around 60 Hz in the chosen frequency range, as depicted in Fig. 5. This behavior is evident when comparing the interharmonic frequencies of the IC and the CBDG under bolted fault conditions, recorded at 60 Hz and 61 Hz, respectively, as shown in Fig. 7. By exploiting these frequency variations, which stem from distinct droop-based no-load frequency limits during faults, the proposed protection scheme effectively detects and isolates faults within the AC subgrid.

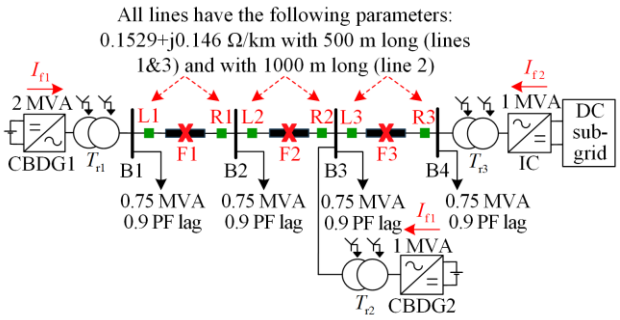



Fig. 6. A simple hybrid AC/DC microgrid layout with integrated proposed differential relays.

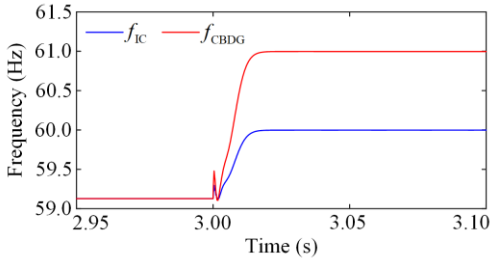



Fig. 7. Frequency response of the IC and CBDG under bolted fault conditions.

### *B. Impact of Bolted Faults on AC Sub-grid*

In hybrid AC/DC microgrids, effectively managing HIFs is essential, particularly in terms of fault resistance. This subsection analyzes the frequency responses of IC and CBDG under varying fault resistances. A single-line-to-ground (SLG) fault occurring at point F2 is considered (refer to Fig. 6), with fault resistances varying between 50 Ω and 100 Ω. Unlike bolted faults, HIFs involve the creation of a high-resistance path at the fault point, which limits the fault current magnitude and delays its propagation. These faults are typically caused by poor contact, insulation failures, or partial conductor damage. The delayed propagation of fault effects, including voltage sags and frequency shifts, can obscure detection mechanisms. The impact spreads slowly across the grid, subtly altering system frequency and voltage profiles, often leading to the miscoordination of traditional protective devices.

As illustrated in Fig. 8, the frequency variation between CBDG and IC decreases as the fault resistance increases, particularly in the 100 Ω case. When the fault resistance exceeds this value, the frequency variation tends to disappear, potentially allowing the CBDG's frequency to drop below 60 Hz and synchronize with the IC's frequency. Accordingly, the proposed protection scheme performs adequately up to a fault resistance of 100 Ω, aligning with the maximum fault impedance typically found in standard distribution systems. Therefore, the algorithm is proficient in identifying faults on the AC side of the grid within this impedance range.

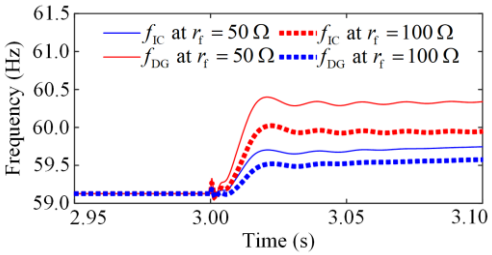



Fig. 8. Frequency response of the IC and CBDG under varying fault resistances.

### *C. Interharmonics Fault Current Generation*

During AC fault conditions, the interaction between the IC and CBDGs results in the superposition of harmonic contributions from multiple sources. This fault-induced interaction creates frequency imbalances between the IC and CBDGs, leading to the generation of interharmonic current components and frequency modulation effects. As a result, interharmonic and subharmonic elements become evident in the system's dynamic response. The propagation of such faults amplifies the coupling dynamics between the IC and CBDGs, posing challenges to the microgrid's stability and complicating the effectiveness of traditional protection methods. However, the proposed protection scheme effectively leverages the frequency variations between the CBDG and IC to detect and isolate faults, including HIFs with resistances up to 100 Ω. To elucidate this concept, a 3-phase bolted fault occurring at point F2 is considered, refer to Fig. 6. The steady-state fault current contributions from CBDG2 and the IC can be mathematically represented as follows:

$$I_{\mathrm{CBDG}_2} = I_{\max}\sin(2\pi f_1 t) \tag{10}$$

$$I_{\mathrm{IC}} = I_{\max}\sin(2\pi f_2 t) \tag{11}$$

where $I_{\max}$ denotes the maximum current limit during fault conditions; while $f_1$ and $f_2$ are the interharmonic frequencies of the fault currents of the $\mathrm{CBDG}_2$ and the IC, respectively. In the bolted fault scenario, $f_1$ for $\mathrm{CBDG}_2$ is 61 Hz, and $f_2$ for the IC is 60 Hz, as referred to in Section III.A. Figure 9(a) shows the sinusoidal waveforms of the fault current contributions from $\mathrm{CBDG}_2$ and the IC. The fault current contributions from $\mathrm{CBDG}_2$ and the IC combine at bus $\mathrm{B}_3$, resulting in the interharmonic fault current measured by $I_{\mathrm{R2}}$, expressed as:

$$I_{\mathrm{R2}} = I_{\max}\sin(2\pi f_1 t) + I_{\max}\sin(2\pi f_2 t) = 2I_{\max}\cos\left(2\pi\frac{f_1 - f_2}{2}t\right)\sin\left(2\pi\frac{f_1 + f_2}{2}t\right) \tag{12}$$

Equation (12) is depicted by the solid black waveform in Fig. 9(b), corresponding to $\sin\left(2\pi\frac{61+60}{2}t\right)$ which

is a 60.5 Hz sine wave (interharmonic current). Moreover, the peak-to-peak amplitude of this 60.5 Hz sinusoid is modulated by $\cos\left(2\pi\frac{61-60}{2}t\right)$ which is a 0.5 Hz cosine wave (sub-harmonic current), resulting in a time-varying amplitude. This paper leverages the behavior and characteristics of the interharmonic current to develop an effective interharmonic current differential protection scheme for fault detection and isolation in the AC subgrid, as explained in the following section.

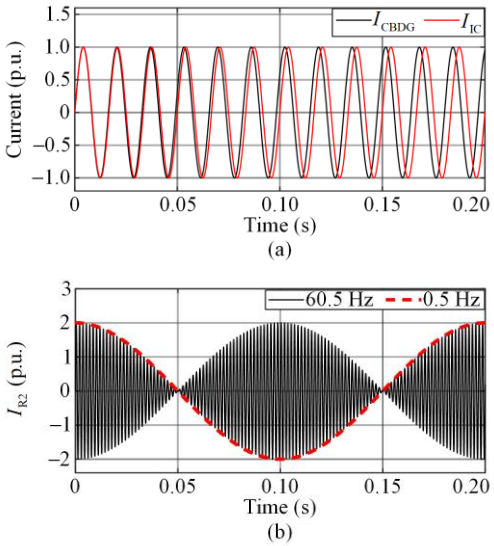



Fig. 9. Fault current waveforms. (a) Individual interharmonic fault currents from $I_{CBDG_2}$ and $I_{IC}$. (b) Combined $I_{R2}$ waveform.

## IV. Proposed Interharmonic Current Differential Protection Scheme

The proposed protection algorithm is designed to operate independently of fault current amplitude, addressing the limitations imposed by fault current limiters in CBDGs during fault conditions. By measuring the interharmonic components of fault currents on both ends of the line, the scheme can accurately identify various types of faults, including HIFs.

### *A. Interharmonic Component Measurement of the Fault Currents*

The scheme utilizes interharmonic frequency variations between ICs and CBDGs in the AC sub-grid during fault conditions due to differing droop-based no-load frequency limits. As detailed in Section III, upon a fault occurrence, the interharmonic frequency of the CBDGs increases to $f_1$, while that of the ICs rises to $f_2$, facilitating fault detection and localization. In the case of an internal fault on the protected line, the interharmonic frequency component of the current at each terminal varies, prompting the scheme to initiate the necessary trip signal. Conversely, during external faults, the interharmonic frequency component of the current is similar at both terminals, rendering the interharmonic current differential relay inactive. Thus, this method effectively identifies internal faults within the protected zone by analyzing the variations in the interharmonic fault current between both ends of the line.

For further illustration, consider the hybrid distribution network depicted in Fig. 6. During a bolted fault, the CBDGs inject an interharmonic current $I_{f1}$ (where $f_1 = 61$ Hz), while the IC injects an interharmonic current $I_{f2}$ (where $f_2 = 60$ Hz). As demonstrated in Fig. 10, the internal fault at F3 causes the relay L3 to detect a fault current ($I_{L3}$) that includes the interharmonic frequency component $I_{f1}$, injected by the CBDGs. Simultaneously, the fault current at the relay $I_{R3}$ incorporates an interharmonic frequency component $I_{f2}$, originating from the IC. Conversely, as illustrated in Fig. 11, an internal fault at F2 leads to the relay L2 detecting a fault current ($I_{L2}$) containing the interharmonic frequencycomponent $I_{f1}$ from CBDG1. The fault current at the relay $I_{R2}$ is characterized by a combination of interharmonic frequency components $I_{f1}$ and $I_{f2}$, as it encompasses currents from both CBDG2 and the IC (refer to Subsection III.B).

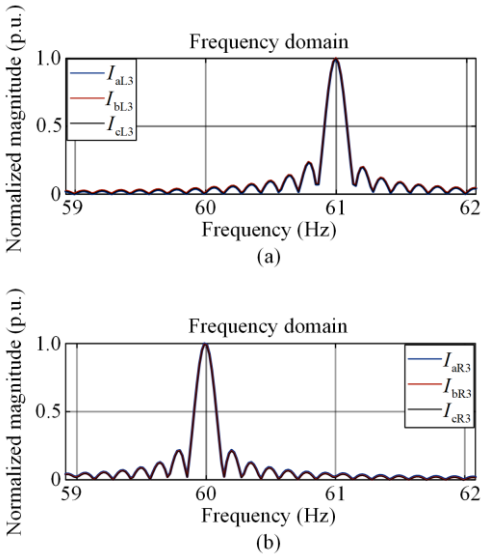
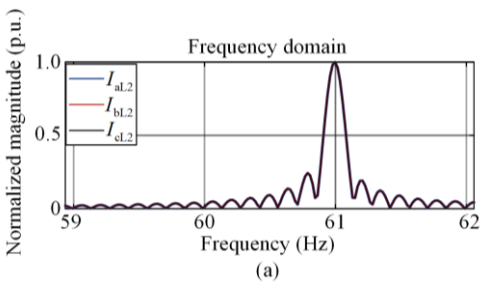



Fig. 10. Frequency domain of the fault currents in the AC subgrid at the bilateral of the faulted line under a bolted 3-phase fault at F3. (a) $I_{L3}$. (b) $I_{R3}$.



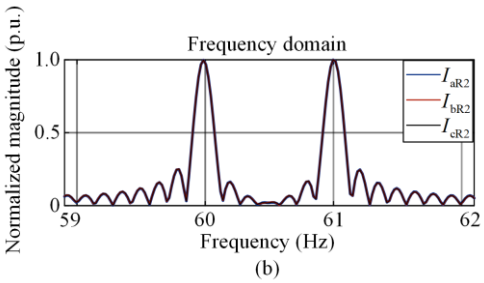



Fig. 11. Frequency domain of the fault currents in the AC subgrid at the bilateral of the faulted line under a bolted 3-phase fault at F2. (a) $I_{L2}$. (b) $I_{R2}$.

*B. The Formulation of the Proposed Differential Scheme*

The proposed interharmonic differential protection scheme is employed to accurately identify and isolate internal faults within a protected zone. This scheme detects internal faults by measuring and comparing the interharmonic fault current components ($I_{f2}$ or $I_{f1}$) at both ends of each line. In the case of an external fault, both relays experience a fault current with identical interharmonic frequency components, thereby no trip signal is triggered. The differential interharmonic frequency component of the current in A, B, and C phases for each relay $i$ is expressed as:

$$I_{\mathrm{diff},i}^{\mathrm{a,b,c}}(f_{2\mathrm{or1}}) = \left| I_{\mathrm{R}i}^{\mathrm{a,b,c}}(f_{2\mathrm{or1}}) - I_{\mathrm{L}i}^{\mathrm{a,b,c}}(f_{2\mathrm{or1}}) \right| \tag{13}$$

where subscripts "R" and "L" are the right-hand side (RHS) and left-hand side (LHS) relays, respectively; and $f_{2\mathrm{or1}}$ represents $f_2$ or $f_1$. The maximum differential interharmonic frequency component of the current is calculated as follows:

$$I_{\mathrm{diff},i}^{\max}(f_{2\mathrm{or1}}) = \max\left\{ I_{\mathrm{diff},i}^{\mathrm{a}}, I_{\mathrm{diff},i}^{\mathrm{b}}, I_{\mathrm{diff},i}^{\mathrm{c}} \right\} \tag{14}$$

where $I_{\mathrm{diff},i}^{\mathrm{a}}$, $I_{\mathrm{diff},i}^{\mathrm{b}}$, and $I_{\mathrm{diff},i}^{\mathrm{c}}$ represent the differential interharmonic components of the current for each relay $i$ in phases A, B, and C, respectively.

As illustrated in Fig. 12, the flow chart of the proposed interharmonic differential relay operation is highlighted, featuring two digital frequency differential relays, R$i$ and L$i$, located on the RHS and LHS, respectively. The initial step in the proposed scheme involves extracting the interharmonic frequency components in the protection criterion from the recorded fault current waveforms using a recursive discrete Fourier transform (R-DFT) at both ends of each line. This scheme qualifies for high-resolution and real-time detection of interharmonics [43]–[46]. The R-DFT method computes signal's spectral components with a satisfactory resolution, enabling the identification of the current interharmonics that are close to the fundamental frequency. This capability is crucial for accurate and effective protection in hybrid microgrids. It allows for the precise identification of interharmonic frequencies, which could indicate potential faults. By optimizing the sampling rate and the number of samples, the protection scheme's sensitivity and response time can be enhanced, thereby improving the detection capability of the proposed protection scheme [46], [47]. Subsequent to this, any undesired frequency components are eliminated. The local and remote end interharmonics frequency components of the currents received via the communication channel, are then utilized at each master differential unit to calculate the differential interharmonic current at each phase $I_{\mathrm{diff},i}^{\mathrm{a,b,c}}$. For each digital relay, the decision to trip is based on the comparison between the maximum differential calculated current $I_{\mathrm{diff},i}^{\max}$ and a predetermined threshold value $I_{\mathrm{diff,th}}$. It is important to note that low bandwidth communication suffices for this operation, as it only requires transferring a small amount of integer measurements using a communication link. The threshold value $I_{\mathrm{diff,th}}$ for the interharmonic differential relay is established based on several critical factors:

1) A measurement error of 1% between the current transformers (CTs) at each end of the line. This adjustment is justified by the implementation of current limiters, which restrict the maximum current to 1.2 times the rated current, thereby effectively reducing the potential errors in CT readings from 10% to 1%, ensuring compliance with IEEE accuracy standards [48];

2) The inclusion of a 5% safety margin to cater for system uncertainties and variations.

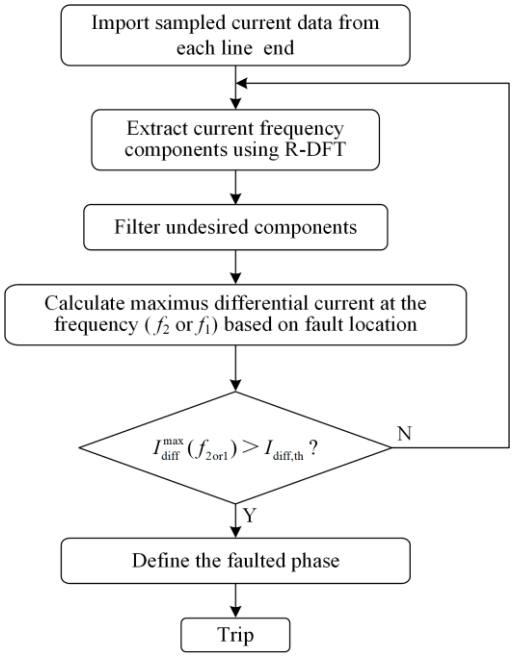



Fig. 12. Flowchart for the proposed protection scheme.

As a result, the proposed differential relay has been configured with a threshold value of 6%, based on the

rated selected frequency current component. To enhance the response time of the protection scheme, the proposed method eliminates frequency components with magnitudes below a specified threshold, avoiding digital filters. This approach minimizes delays, ensuring a quicker and more effective protection scheme. The next section will focus on assessing the performance of this protection algorithm using example networks.

## V. Performance Assessment

In this section, the performance of the proposed protection algorithm is assessed using two systems: a modified 4-bus hybrid microgrid derived from a segment of the Canadian urban distribution system, and a modified islanded IEEE33-bus hybrid AC/DC microgrid equipped with CBDGs. A sensitivity analysis is conducted to evaluate the algorithm's effectiveness under various fault conditions, including different fault locations, types, and HIFs.

### *A. 4-bus Canadian Urban Hybrid Microgrid*

The 4-bus hybrid microgrid, shown in Fig. 6, is a modified segment of the Canadian urban distribution benchmark system, designed to operate as an islanded hybrid AC/DC microgrid. This microgrid is supplied by two CBDGs and is connected to a DC sub-grid through an IC. These DGs are linked to the AC distribution network through 600 V/12.67 kV power transformers and the entire system is modeled and simulated on PSCAD/EMTDC. Both CBDGs and the IC utilize hard limiters to restrict their output currents to 1.2 times their rated currents. In response to the variability of fault resistance based on fault type, location, and environmental conditions [49], a realistic range of fault resistance values is incorporated to enhance the accuracy of the simulations. As illustrated in Fig. 13, fault types in the microgrid are categorized as ground faults, i.e., three line-to-ground (3LG), double-line-to-ground (DLG) and single-line to-ground (SLG); and phase faults, i.e., double-line (DL) and three-phase. To align with typical values observed in power systems, line-to-ground faults are modeled with resistance ($r_{\mathrm{f}}$) values ranging from 0.1 Ω to 100 Ω.

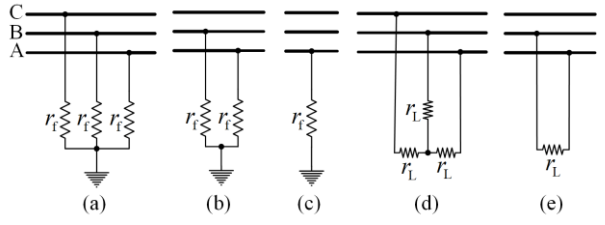


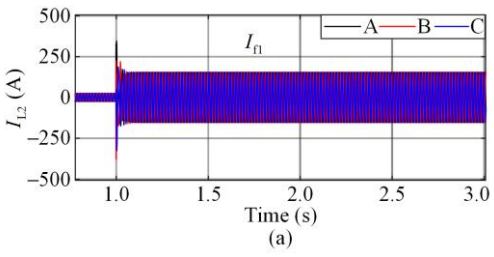

Fig. 13. Fault representation in microgrid. (a) Three-phase-to-ground fault. (b) Double-line-to-ground fault. (c) Single-line-to-ground fault. (d) Three-phase fault. (e) Double-line fault.

This range accounts for high-resistance scenarios, such as contact with vegetation or soil. For line-to-line and three-phase faults, a lower resistance range of 0.1 Ω to 10 Ω ($r_{\mathrm{L}}$) is applied, representing the generally low-impedance nature of these fault types. This expanded range is designed to capture realistic fault conditions and test the maximum detectable fault resistance using the proposed algorithm.

To assess the effectiveness of the suggested protection scheme with different fault locations, two 3-phase faults are initiated at locations F2 and F3, refer to Fig. 6, occurring at $t = 1$ s. The corresponding results for both fault locations are presented in Table I, detailing the relay currents at both ends for each phase. Moreover, Figs. 14 and 15 illustrate the fault currents for the three phases at both ends, considering fault locations F2 and F3, respectively. At the fault instant, CBDG1 and CBDG2 inject interharmonic currents of 61 Hz ($I_{\mathrm{f1}}$), while the IC injects an interharmonic current of 60 Hz ($I_{\mathrm{f2}}$), as illustrated in Section IV.A. The interharmonic frequency current component of the IC ($I_{\mathrm{f2}}$) is utilized at both ends of each line for fault detection, as explained in subsection IV.B. The differential interharmonic current for each phase $I_{\mathrm{diff},i}^{\mathrm{a,b,c}}(f_2)$ is shown in the last column of Table I. The maximum differential interharmonic currents $I_{\mathrm{diff},i}^{\max}(f_2)$, based on Eq. (14), are compared with the threshold ($I_{\mathrm{diff,th}} = 0.06 \times I_{\mathrm{IC,rated}} = 2.75$ A) for each relay. A trip signal is triggered for both fault locations if the values of the maximum differential interharmonic currents exceed this predefined threshold.

TABLE I
Relay Currents for Different Fault Locations for 4-bus Hybrid AC/DC Microgrid

| Fault location | Fault type | Phase | SE (A) | | | RE (A) | | | $I_{\mathrm{diff},i}^{\mathrm{a,b,c}}$ |
|---|---|---|---|---|---|---|---|---|---|
| | | | $I_{\mathrm{L}i}$ | $I_{\mathrm{f2}}$ | $I_{\mathrm{f1}}$ | $I_{\mathrm{R}i}$ | $I_{\mathrm{f2}}$ | $I_{\mathrm{f1}}$ | $I_{\mathrm{f2}}$ |
| F2 | 3LG | A | $I_{\mathrm{L2}}$ | 0 | 109.4 | $I_{\mathrm{R2}}$ | 54.7 | 54.7 | 54.7 |
| | | B | | 0 | 109.4 | | 54.7 | 54.7 | 54.7 |
| | | C | | 0 | 109.4 | | 54.7 | 54.7 | 54.7 |
| F3 | 3LG | A | $I_{\mathrm{L3}}$ | 0 | 164 | $I_{\mathrm{R3}}$ | 54.7 | 0 | 54.7 |
| | | B | | 0 | 164 | | 54.7 | 0 | 54.7 |
| | | C | | 0 | 164 | | 54.7 | 0 | 54.7 |



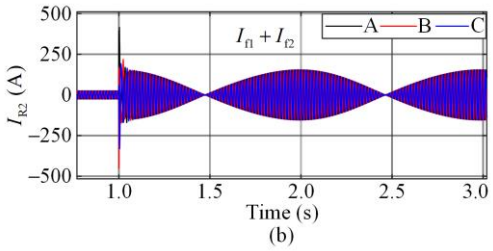



Fig. 14. The fault currents in the AC subgrid at the bilateral of the line under bolted 3-phase fault at F2. (a) $I_{L2}$. (b) $I_{R2}$.

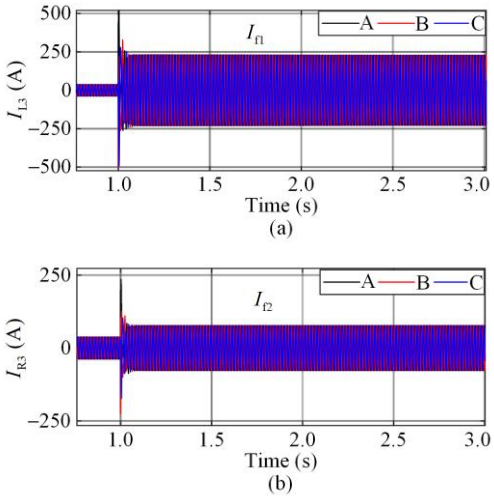



Fig. 15. The fault currents in the AC subgrid at the bilateral of the line under bolted 3-phase fault at F3. (a) $I_{L3}$. (b) $I_{R3}$.

Additionally, Table II provides a comprehensive overview, summarizing the observed interharmonic current components of the IC ($I_{f2}$), measured by the relays (L3 and R3) at the ends of line 3 under different types of faults at F3, and for both low and high fault resistances ($r_f = 0.1\ \Omega$ and $r_f = 100\ \Omega$). The last column of this table displays the differential current for each phase, denoted as $I^{a,b,c}_{diff,i}(f_2)$. The differential relay compares the maximum differential interharmonic current $I^{max}_{diff,i}(f_2)$ with the threshold value $I_{diff,th} = 2.75$ A, generating a trip signal once $I^{max}_{diff,i} > I_{diff,th}$. For fault classification, the differential interharmonic current of each phase $I^{a,b,c}_{diff,i}(f_2)$ is compared with a pre-established threshold to identify the phases affected by the fault.

TABLE II
RELAY CURRENTS AT DIFFERENT FAULT TYPES AND RESISTANCES AT F3 FOR 4-BUS HYBRID AC/DC MICROGRID

| Fault location | Fault type | Phase | Relay currents ($I_{f2}$), $I_{diff,th} = 2.75$ A | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | $r_f / r_L = 0.1\ \Omega / 0.1\ \Omega$ | | | $r_f / r_L = 100\ \Omega / 10\ \Omega$ | | |
| | | | $I_{L3}$ (A) | $I_{R3}$ (A) | $I^{a,b,c}_{diff,i}$ (A) | $I_{L3}$ (A) | $I_{R3}$ (A) | $I^{a,b,c}_{diff,i}$ (A) |
| F3 | 3LG | A | 0 | 54.7 | 54.7 | 27.3 | 54.7 | 27.4 |
| | | B | 0 | 54.7 | 54.7 | 27.3 | 54.7 | 27.4 |
| | | C | 0 | 54.7 | 54.7 | 27.3 | 54.7 | 27.4 |
| | A-B-G | A | 5.5 | 54.7 | 49.2 | 26.4 | 54.7 | 28.3 |
| | | B | 8.2 | 54.7 | 46.5 | 26.5 | 54.7 | 28.2 |
| | | C | 53 | 53 | 0 | 54.7 | 54.7 | 0 |
| | A-B | A | 10.9 | 54.7 | 43.8 | 30.1 | 54.7 | 24.6 |
| | | B | 13.6 | 54.7 | 41.1 | 30.1 | 54.7 | 24.6 |
| | | C | 47 | 47 | 0 | 54.7 | 54.7 | 0 |
| | A-G | A | 2.73 | 54.7 | 51.9 | 27 | 54.7 | 27.7 |
| | | B | 54.7 | 54.7 | 0 | 54.7 | 54.7 | 0 |
| | | C | 54.7 | 54.7 | 0 | 54.7 | 54.7 | 0 |

### *B. IEEE33-bus Islanded Hybrid Distribution System*

The proposed algorithm is further evaluated using a modified version of the IEEE33-bus islanded hybrid microgrid, illustrated in Fig. 16.

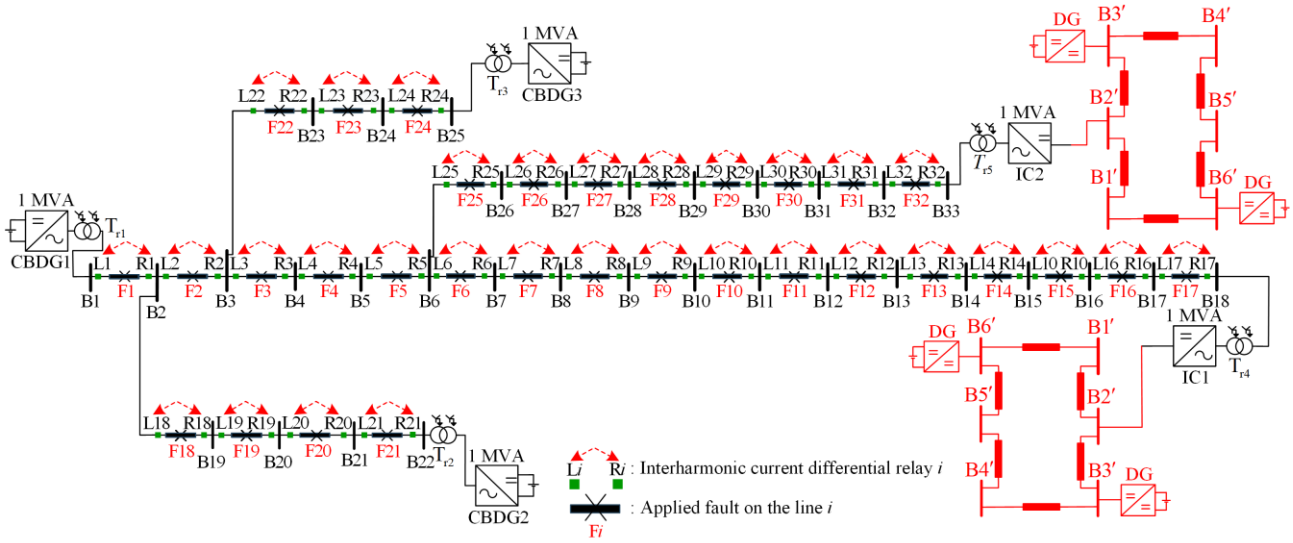



Fig. 16. Modified IEEE33-bus hybrid AC/DC distribution system.

The data of the loads and system's lines can be found in [40], [50]. The ratings and locations of the CBDGs and ICs are detailed in [51]. Each CBDG and IC is rated at 1 MVA and linked through a 600 V/12.67 kV power transformer. The modeling of the system is conducted using PSCAD/EMTDC. the simulation parameters, including the sampling time, are indicated in Table III. To ensure safe operation, the current hard limiter value is set at 1.2 p.u. for all CBDGs and ICs. As illustrated in Fig. 16, the fault locations in the middle of each system line are identified by the symbols F1–F32. The proposed scheme incorporates interharmonic current differential relays positioned at both ends of each line section for detecting and isolating the faulted line.

TABLE III
PSCAD SIMULATION PARAMETER

| Parameter | Value |
|---|---|
| Sampling time (μs) | 50 |
| Simulation duration (s) | 10 |
| Solver type | EMTDC solver |
| Step size (μs) | 100 |
| Nominal grid voltage (kV) | 12.67 |
| System frequency (Hz) | 60 |
| Converter switching frequency (kHz) | 10 |

Table IV illustrates the interharmonic frequency components of the fault current at both ends (L*i* and R*i*) of the faulted lines in the AC sub-grid, considering various fault locations and types for both low and high fault resistances ( $r_f/r_L = 0.1\ \Omega/0.1\ \Omega$ and $r_f/r_L = 100\ \Omega/10\ \Omega$ ). For faults occurring between CBDGs and ICs, or within CBDGs on both sides and the IC on one side (e.g., F1–F5, F18–F21, F22–F24), the interharmonic frequency componentsmof fault currents ($I_{f2}$) from the ICs at both line ends are used in the proposed scheme to calculate the differential current. For instance, in a single line-to-ground (A-G) fault at F1, the fault current magnitudes in phase A, represented by $I_{L1}$ and $I_{R1}$, are 10.9 A and 109.4 A, respectively. The proposed scheme calculates the differential current for each phase, denoted as $I_{diff,i}^{a,b,c}(f_2)$. The maximum differential current $I_{diff,i}^{max}(f_2)$, according to Eq. (14), are compared with the predetermined threshold value $I_{diff,th}$, set to ($0.06 \times I_{IC,rated} = 2.75$ A) (as referenced in subsection IV.B). Since $I_{diff,1}^{max} = 82$ A exceeds $I_{diff,th} = 2.75$ A, a relay 1 trip signal is triggered. Additionally, for the same fault at F1, the differential currents in phases B and C are zero, confirming the fault as a single line-to-ground (A-G) fault in phase A.

TABLE IV
RELAY CURRENTS AT DIFFERENT FAULT TYPES, LOCATIONS AND RESISTANCES FOR 33-BUS HYBRID AC/DC MICROGRID

| | Fault location | Fault type | Phase | $r_f/r_L = 0.1\ \Omega/0.1\ \Omega$ | | | $r_f/r_L = 100\ \Omega/10\ \Omega$ | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $I_{Li}$ (A) | $I_{Ri}$ (A) | $I_{diff,i}^{a,b,c}$ (A) | $I_{Li}$ (A) | $I_{Ri}$ (A) | $I_{diff,i}^{a,b,c}$ (A) |
| Relay currents ($I_{f2}$), $I_{diff,th} = 2.75$ A | F1 | A-G | A | 10.9 | 109.4 | 98.5 | 27.4 | 109.4 | 82 |
| | | | B | 54.7 | 54.7 | 0 | 33 | 33 | 0 |
| | | | C | 27.4 | 27.4 | 0 | 33 | 33 | 0 |
| | F2 | A-B-G | A | 21.9 | 109.4 | 87.5 | 38.3 | 76.6 | 38.3 |
| | | | B | 27.4 | 109.4 | 82 | 38 | 82 | 44 |
| | | | C | 66 | 66 | 0 | 46 | 46 | 0 |
| | F4 | A-B | A | 28.4 | 109.4 | 81 | 56.9 | 85.3 | 28.4 |
| | | | B | 38.3 | 109.4 | 71.1 | 54.7 | 93 | 38.3 |
| | | | C | 93 | 93 | 0 | 76.6 | 76.6 | 0 |
| Relay currents ($I_{f1}$), $I_{diff,th} = 8.25$ A | F8 | 3LG | A | 164 | 0 | 164 | 164 | 106.6 | 57.4 |
| | | | B | 164 | 0 | 164 | 164 | 106.6 | 57.4 |
| | | | C | 164 | 0 | 164 | 164 | 106.6 | 57.4 |

Conversely, for faults between ICs on both sides and CBDGs on one side (e.g., F6–F17 and F25–F32), the scheme considers the interharmonic frequency components of the fault currents ($I_{f1}$) from the CBDGs at the two line ends in the AC subgrid when calculating the differential interharmonic current. Selecting the CBDG's interharmonic frequency ($f_1$) components of the fault current ensures accurate fault detection and classification in scenarios involving faults between two ICs. For instance, in the event of a three-line-to-ground (3LG) fault occurring at F8 with a HIF of $r_f = 100\ \Omega$. It is inotable that the interharmonic fault current components ($I_{f1}$) in phases A, B, and C differ on both sides of the faulted line, denoted by $I_{L8}$ and $I_{R8}$, with values of 164 A and 106.6 A, respectively. The proposed protection scheme utilizes these current magnitudes by calculating their difference and subsequently comparing the maximum differential current, $I_{diff,8}^{max}$, with a predetermined threshold value, $I_{diff,th}$. In this case, the threshold value, $I_{diff,th}$, is determined as $0.06 \times 3I_{CBDG,\ rated} = 8.25$ A, as described in subsection IV.B. Since $I_{diff,8}^{max} = 57.4$ A,

which is greater than the threshold value of $I_{\text{diff,th}} = 8.25$ A, a trip signal for relay 8 is triggered. Furthermore, the fault type is conclusively identified as a 3LG fault. Table IV demonstrates that the highlighted $I_{\text{diff},i}^{\max}$ is higher than $I_{\text{diff,th}}$ for all fault locations and types, including HIFs ($r_{\text{f}}/r_{\text{L}} = 100\ \Omega/10\ \Omega$). According to the R-DFT analysis, it is observed that the computational time remains consistent across various fault types, with a fixed duration of 25 ms. Moreover, the communication delay is approximately 20 ms [21], [52]. Consequently, the overall trip time is estimated to be approximately 45 ms. The presented case studies underscore the scheme's effectiveness in enhancing fault detection, selection, and classification, thus ensuring reliable protection for the AC side of the islanded hybrid AC/DC microgrid.

### *C. Comparative Evaluation*

To conduct a comparative study, the modified IEEE33-bus hybrid distribution system shown in Fig. 16 is equipped with the current line differential relays proposed in [53], [54]. A single-line-to-ground fault (A-G) at location F4 is introduced considering various fault resistances ($r_{\text{f}}$) of 5 Ω, 10 Ω, and 50 Ω, respectively. Figure 17 displays the root-mean-square (RMS) differential phase currents at both ends of the line segment 4–5 utilizing current-based differential protection. As can be seen, the proposed protection scheme and the current-based differential protection scheme can detect the internal fault with $r_{\text{f}} = 5\ \Omega$. On the other hand, the current-based differential protection scheme fails to detect an internal fault with $r_{\text{f}} = 10\ \Omega$ and $r_{\text{f}} = 50\ \Omega$ since the RMS differential current for phase A remains within the differential relay threshold. On the contrary, based on results in Section V.B, the proposed interharmonic current differential relay is capable of detecting faults with impedance up to 50 Ω.

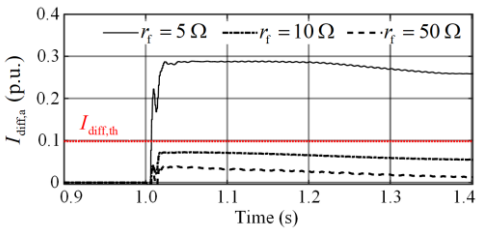



Fig. 17. Simulation results during SLG fault at F4 for different fault resistances with the current-based differential protection scheme.

It is important to note that implementing the proposed protection scheme can impose several challenges. First, it is applicable to islanded hybrid AC/DC microgrids with CBDGs since it will be very difficult to equip such a proposed scheme with synchronous-based DGs, as it is tailored to the unique characteristics of CBDG and IC. Besides, the proposed method relies on the differential concept, which requires the availability of communication.

## VI. Experimental Validation using HIL Setup

The performance of the proposed interharmonic differential protection scheme is further evaluated using a real-time HIL experimental setup, as outlined in Fig. 18. The hybrid converter-based islanded microgrid, shown in Fig. 6, is converted from PSCAD to RSCAD software to be compatible with the real-time digital simulator (RTDS) environment. The utilized RTDS processing hardware model is a NovaCor 2.0 with 10 cores operating at 3.8 GHz. The phase current waveforms at both line ends are sampled at 20 kHz (every 50 μs) and exported to the NI-MyRio interface card, utilizing the GTAO card within the RTDS. The proposed protection scheme is implemented in LabVIEW to evaluate the current measurements and generate a trip signal in case a fault occurs. If a trip signal is issued, it is returned to the RTDS using the NI-myRIO device and GTDI card, thus completing the HIL setup. For monitoring the trip signal from NI-MyRIO as well as the current waveforms from RTDS, a Tektronix-DPO4054B oscilloscope is used to monitor and calculate the real-time required for the proposed protection scheme.

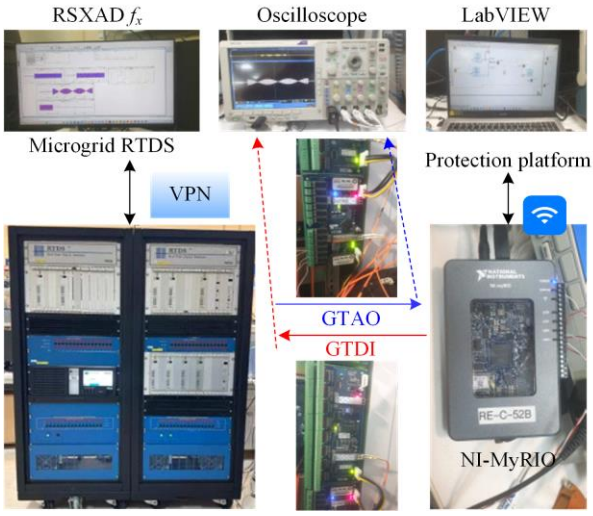



Fig. 18. HIL experimental setup using RTDS.

A 3LG fault is initiated at F2, refer to Fig. 6, occurring at $t = 1$ s. The three-phase current waveforms at both line ends are presented in Fig. 19. The protection scheme is initiated in LabVIEW software after evaluating the current waveforms and initiating the trip signal in case of a fault occurrence. The detection process involves continuously monitoring the phase current waveforms and calculating the differential current $I_{\text{diff},i}^{\max}$. Since in the fault case the $I_{\text{diff},i}^{\max}$ exceeds the

threshold value $I_{\text{diff,th}}$, a trip command is issued to isolate the fault. This trip command is generated within 28 ms after the fault instant, as shown in Fig. 20. The prompt trip response confirms the efficient performance and reliability of the proposed protection scheme when tested using the real-time HIL setup. The HIL setup provides a robust platform to validate the practical applicability and effectiveness of the protection scheme in handling actual fault scenarios.

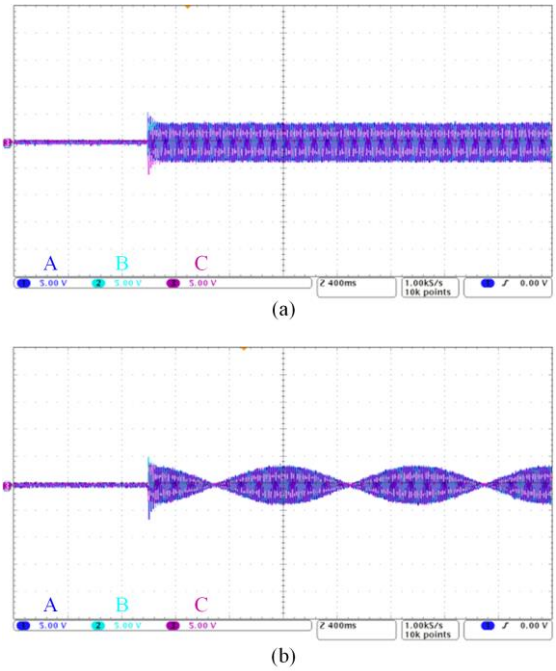



Fig. 19. The real-time fault currents at the bilateral of the line under 3-phase fault at F2. (a) $I_{\text{L2}}$. (b) $I_{\text{R2}}$.

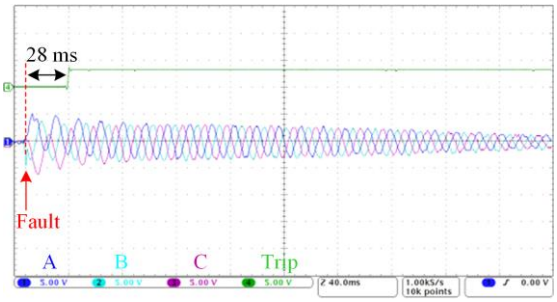



Fig. 20. Trip command after the fault instant at F2 for bolted 3LG fault.

## VII. Conclusion

This paper introduces an innovative interharmonic current differential protection algorithm for the AC side of hybrid AC/DC islanded microgrids with CBDGs. The proposed scheme effectively addresses the challenge related to limited CBDG fault currents by exploiting the interharmonic frequency difference between IC and CBDGs during faults to detect and isolate AC side faults in hybrid microgrids. Interharmonic Differential relays are located at each end of the distribution lines to provide fault detection, isolation, and classification. The effectiveness of the proposed scheme is demonstrated using PSCAD/EMTDC simulations on a 4-bus Canadian Urban distribution system and a modified IEEE33-bus hybrid AC/DC distribution system. The simulation results highlight the proposed protection scheme's effectiveness in detecting various fault types, locations, and resistances up to 100 Ω. Furthermore, a comparative study is conducted, highlighting the significance of the proposed protection scheme. The effectiveness of the proposed protection scheme is further validated through a comprehensive real-time HIL experimental setup, demonstrating its practical applicability and reliability. The proposed scheme offers a promising solution for protecting hybrid AC/DC islanded microgrids with CBDGs, ensuring reliable operation and enhancing system performance.

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## Authors' Contributions

Ahmed Abdelemam: conceptualization, software, validation, investigation, writing original draft, writing review & editing, visualization, methodology, and formal analysis. Hatem Zeineldin: conceptualization, validation, writing review & editing, methodology, and supervision. Ahmed Al-Durra and Ehab El-Saadany: conceptualization, validation, writing review & editing, and supervision. All authors read and approved the final manuscript.

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## Availability of Data and Materials

Not applicable.

## Declarations

Competing interests: The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this article.

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