A Novel High-boost Interleaved DC-DC Converter for Renewable Energy Systems

Yin Chen, Haibin Li, and Tao Jin, *Senior Member*, *IEEE*

***Abstract*—A high-boost interleaved DC-DC converter that utilizes coupled inductors and voltage multiplier cells (VMC) is proposed in this paper. The input power supply connects to switches through the primary sides of two coupling inductors with an interleaved structure, which reduces the voltage stresses of the switches and lowers the input current ripple. Two capacitors and a diode are placed in series on the secondary side of the coupled inductors to enhance the high boost capability. The implementation of maximum power point tracking (MPPT) is facilitated by the simplification of the control system through common ground. To verify the effectiveness of the proposed converter, an experimental platform and a prototype based on a turns ratio of 1 are presented. The test results show that the voltage stresses on the switches are only 1/8 of the output voltage. The operating principle and design guidelines of the proposed converter are described in detail. The experimental results show that the converter is efficient and stable over a wide power range.**

***Index Terms*—High voltage gain, DC-DC converter, coupled inductor, low voltage stress.**

I. INTRODUCTION

With the intensification of global warming and environmental pollution, the disadvantages of fossil energy have become obvious. The proposal of reducing carbon dioxide emission and achieving carbon neutrality has accelerated the speed of energy low-carbon transformation [1]. The use of renewable energy is a very effective means of reducing carbon emissions. Renewable energy has characteristics of sustainability, cleanliness, and often, inexhaustible supply [2]. Renewable energy sources generally have low output voltages, such as photovoltaics (PVs) and fuel cells (FCs). Thus, converters are important equipment used to connect renewable energy sources whose output voltage is typically low (20 V–50 V) to the grid, as shown in Fig. 1. One efficient way to meet this high output voltage requirement is to use PVs or FCs series stacking modules. The other method to boost this voltage to a level sufficient for grid connection is to use efficient high-boost DC-DC converters, which regulate the voltage onto the DC bus (400 V or 800 V) [3], [4].

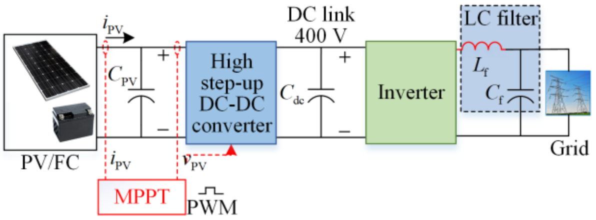

Fig. 1. Photovoltaic and fuel cell grid-connected system diagram.

Various types of high-boost DC-DC converters have been proposed. The voltage-boosting techniques widely adopted include switching capacitor (SC), switching inductor (SL), cascade connection, and coupled inductor (CI) techniques using either conventional or interleaved boost converters to step up the voltage gain. However, conventional boost converters are less commonly used due to their high switch voltage stress and insufficient boost capability [5]. SL has limited boosting capability, while SC generates current surges [6], [7]. Cascading boost units can increase the output voltage, but it is important to consider the potential impact on the system's stability [8], [9]. The method of integrating coupled inductor technology with other technologies has attracted many attentions, and the appropriate voltage gain can be achieved by adjusting the proper turns ratio [10].

Among the introduced techniques, some structures of high-boost converters are single switch boost converters [11]–[15]. For instance, the topology proposed in [15] is composed of two hybrid voltage multiplier cells (VMC), a three-winding coupled inductor, and a single switch. Although the single switch provides a higher voltage gain, the input current ripple of this type of converter is large, while low input current ripple can simplify MPPT and extend the life of the input power supply. Conventional interleaved parallel converters have low boost capability and the switch voltage stress is equal to the output voltage. In recent years, several interleaved high step-up converters based on various techniques have been introduced to reduce input current ripple.

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In [16], the proposed converter utilizes clamp capacitors and integrates a secondary winding with an integrated transformer. Therefore, it achieves high voltage gain for power devices and lower voltage stress. However, the diode voltage stress remains equal to the output voltage. In [17], a super high-boost converter is proposed, including a switched capacitor unit and stacked coupled inductors. The voltage gain can be increased by using a stacking approach and adjusting the turns ratio of the coupled inductors on the output side. However, this may lead to poor stability of the output voltage due to multiple capacitors in series, resulting in larger output voltage ripple. In [18], a novel interleaved DC-DC converter is proposed that successfully integrates an asymmetric voltage multiplier cell (AVMC) with coupled inductors. In [19] and [20], two hybrid cascaded boost converters are proposed, composed of modules derived from the basic boost unit connected in a series-parallel interleaved manner to achieve super high voltage gain, lower input ripple current and output voltage ripple, as well as ultra-low distributed voltage stress on power devices. In [21], an interleaved non-isolated DC-DC converter applying the interleaving technique is proposed to reduce input current ripple. By fully utilizing the leakage inductance of the coupled inductor, the diode is turned off under zero current switching conditions. Reference [22] proposes a TW-CI based on a cascaded high-boost converter with interleaving, which greatly improves the boosting capability. This results in significantly lower voltage stress on the semiconductor compared to the output voltage. However, the input and output voltages do not share a common ground, which can significantly increase the risk of leakage current and complicate the control system. References [23] and [24] propose several converters that use coupling inductors to construct resonant supercharging and achieve lower input current ripple. However, the voltage gain is not significantly improved and the topological voltage gain equation includes a duty cycle parameter leading to relatively complex control.

In [25], the converter with a boost expansion at the front end is presented, which achieves a higher gain range, whereas the converters proposed in [26]–[28] also offer valuable insights worth considering. However, these topologies do not offer significant advantages in terms of voltage gain and efficiency. Based on the above analyses, a novel high-boost interleaved DC-DC converter is proposed in this paper, as shown in Fig. 2. The converter is built using the coupled-inductor technique, the voltage clamp circuit, and VMC, where the VMC capacitor is connected in series with the secondary windings of the coupled inductors. The proposed converter offers several advantages:

1) Higher voltage gain is obtained due to the active clamp circuit participating in voltage step-up, and the stresses in the circuit are distributed.

2) Lower input current ripple due to the interleaved structure, and the efficiency is significantly increased.

3) A common ground is provided between the input and output voltages.

The organization of this paper is as follows. In Section II, the proposed converter and its operating principles are presented, and the modes of this topology are analyzed. In Section III, steady-state analysis is performed and the gain formula and stress formulas of other devices are obtained. In Section IV, the design guidelines are discussed, whereas in Section V, experimental verification with a design example is presented. Finally, Section VI draws the conclusion.

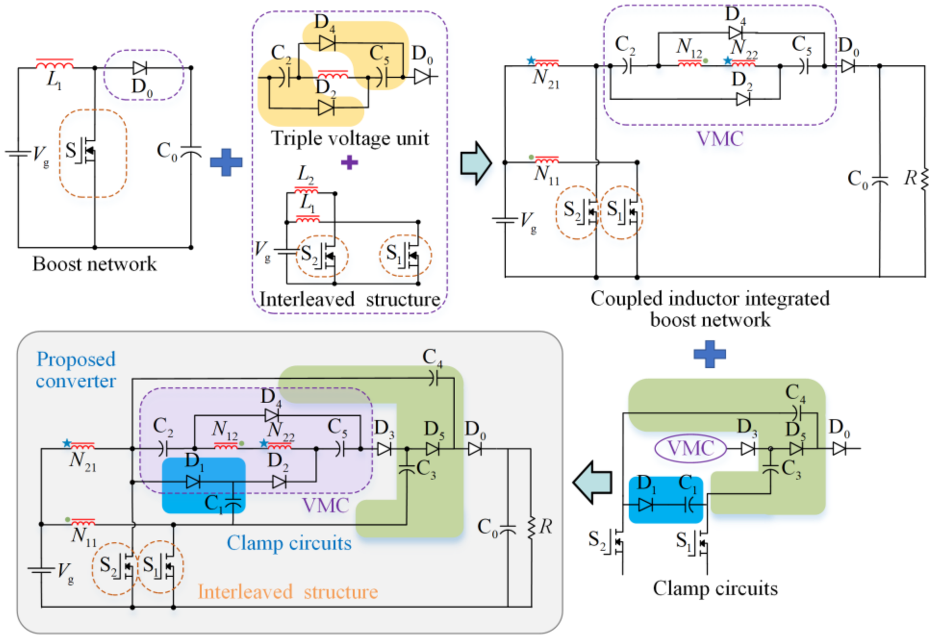


Fig. 2. Derivation of the proposed converter.

II. PROPOSED CONVERTER AND OPERATION PRINCIPLES

The derivation process of the proposed converter is illustrated in Fig. 2. This topology integrates triple voltage cells and a boost circuit with an interleaved structure. By utilizing two interleaved power switches, the current stress is distributed among the switches. Additionally, the converter employs two clamping circuits to reduce switch voltage spikes.

The proposed topology is further shown in Fig. 3. There are two coupled inductors which are defined by ideal transformers with magnetizing inductors (L_{m1} and L_{m2}) and leakage inductors (L_{k1} and L_{k2}). The coupled inductors have primary windings (N_{11} and N_{21}) with N_1 turns, and their secondary windings (N_{12} and N_{22}) with N_2 turns. The secondary inductors N_{12} and N_{22} are connected in series with the switched capacitor to VMC. The turns ratio of the coupled inductors is equal to $n = N_2/N_1$.

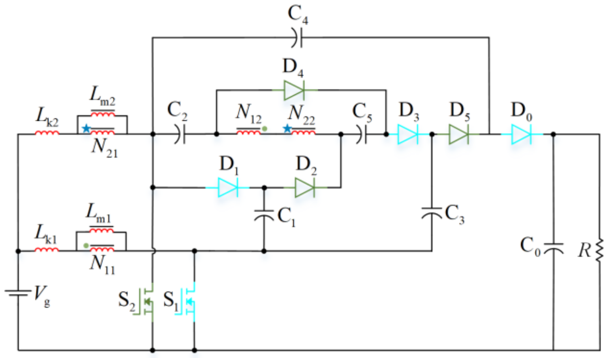


Fig. 3. Power circuit of the proposed converter.

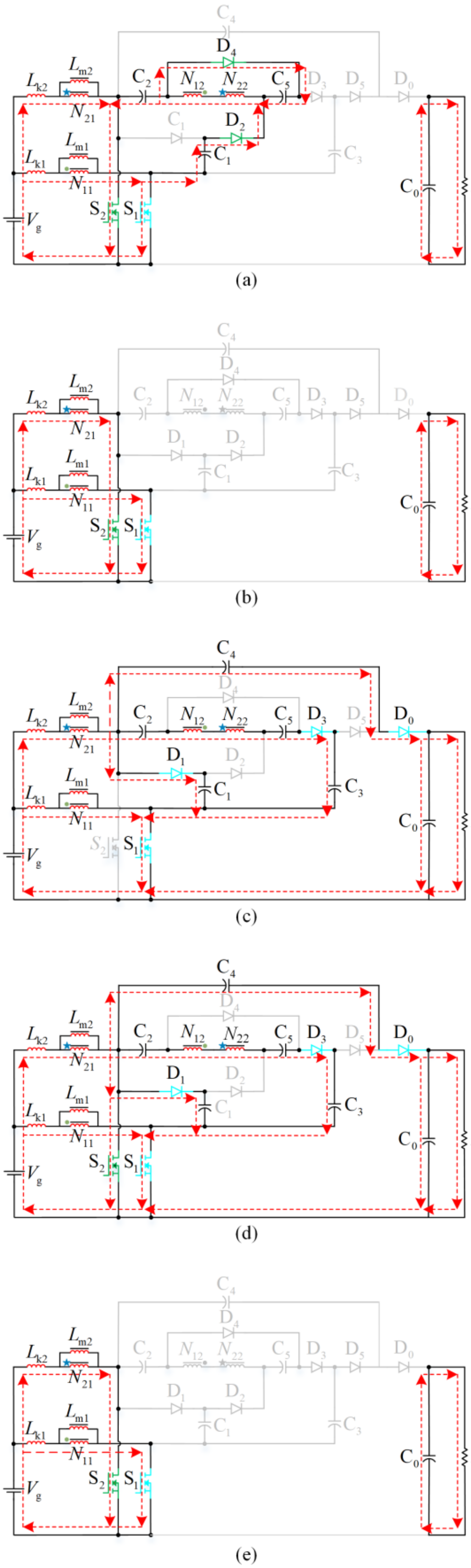
The duty cycle of the switches (S_1 and S_2) is more than 0.55, while the operating phase of switch S_2 in the converter is lagged behind S_1 by 180º. There are six diodes D_1, D_2, D_3, D_4, D_5, and D_0; and six capacitors C_1, C_2, C_3, C_4, C_5, and C_0 in this topology. To simplify the operating principles analysis, there are some assumptions as follows:

1) All semiconductors and diodes are ideal devices, and the on-resistance is zero, and there is no forward voltage drop.

2) The magnetizing inductance is large enough to ensure that the operation of the converter is in continuous conduction mode (CCM).

3) The capacitance is large enough to keep the capacitor voltage stable. And the equivalent series resistances of the inductors and capacitors are zero.

Although the above assumptions exist, the switch and diode on/off processes are instantaneous. The four operating modes within one switching period are illustrated in Fig. 4. The waveforms of the proposed converter operating in steady-state are depicted in Fig. 5.



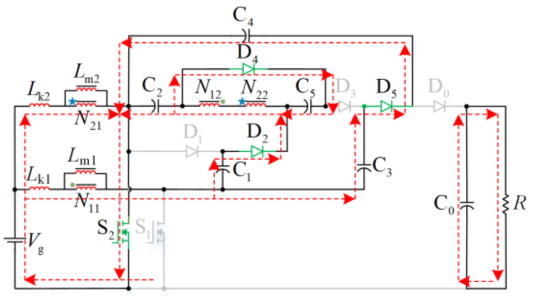
(a)

(b)

(c)

(d)

(e)



(f)

Fig. 4. Operating modes of the proposed converter. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI.

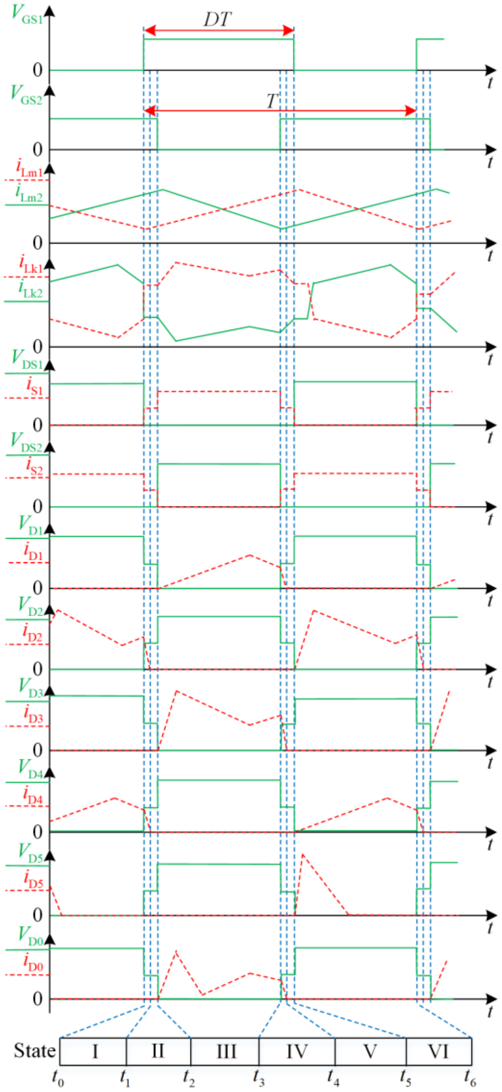


Fig. 5. Key waveforms of the proposed converter.

Mode I [t_0 , t_1]: At time t_0 , switches S_1 and S_2 are turned on in the previous cycle. At this moment, capacitors C_4 and C_3 have already completed charging and stabilized, hence diode D_5 is in the off state, and load R is powered by C_0 , as shown in Fig. 4(a). During this time interval, the voltages on both sides of N_{11} and N_{21} tend to be the same, but a small voltage difference still causes currents to flow through D_4 and D_2 . It is only after the current drops below the diode cut-off current that the currents through D_2 and D_4 will be zero, entering the next mode.

Mode II [t_1 , t_2]: At time t_1 , S_1 and S_2 have been on for some time, and the voltages of N_{11} and N_{21} are equal. The equivalent circuit is shown in Fig. 4(b), where the magnetizing inductors (L_{m1} and L_{m2}) and leakage inductors (L_{k1} and L_{k2}) are charged by the input voltage source V_g . Load R continues to be powered by C_0 .

$$i_{\mathrm{Lm1}}(t)=i_{\mathrm{Lm1}}(t_0)+\frac{V_g}{L_{m1}+L_{k1}}t \tag{1}$$

$$i_{\mathrm{Lm2}}(t)=i_{\mathrm{Lm2}}(t_0)+\frac{V_g}{L_{m2}+L_{k2}}t \tag{2}$$

Mode III [t_2 , t_3]: At the beginning of the mode, switch S_2 is turned off and switch S_1 is still in on state. Diodes D_1 , D_3 , and D_0 are turned on, but D_2 , D_4 and D_5 are blocked. Inductor L_{m1} absorbs energy from the power source V_g through S_1 . Inductor L_{m2} transfers energy to C_1 via D_1 and S_1 , while the voltage across S_2 is clamped to the voltage of C_1 . Thus, the voltage difference between the two sides of C_1 decreases. Capacitor C_3 gets energy from L_{m2} , C_2 , C_5 , N_{12} , N_{22} , and S_1 , while capacitor C_4 is connected in series to transfer energy to C_0 and R via D_0 . The current flow path is depicted in Fig. 4(c).

Due to the existence of the parasitic capacitance, the current of inductors L_{m2} and L_{k2} starts to charge switch S_2 at t_2 , the voltage across switch S_2 will delay and finally reach the maximum value in the time interval.

$$V_{S2}(t)=\frac{i_{\mathrm{Lm2}}(t)}{C_{\mathrm{S2\_self}}}(t-t_2) \tag{3}$$

$$i_{D3}(t)=\frac{1}{n}\left(i_{\mathrm{Lm2}}(t)-i_{\mathrm{Lk2}}(t)\right) \tag{4}$$

Mode IV [t_3 , t_4]: At the beginning of this mode, S_1 remains on while S_2 starts to conduct, as shown in Fig. 4(d). The voltage across S_2 decreases, causing the voltage on the capacitor of S_2 to be discharged and form a conducting current. Due to the drain-source voltage of S_2 , diodes D_1 , D_3 , and D_0 continue to conduct until S_2 stabilizes and eventually are turned off. C_0 will continue to briefly charge until entering the next mode.

Mode V [t_4 , t_5]: In this mode, both S_1 and S_2 are on and all diodes are off, the capacitors' charges are maintained in a transient peak state, waiting for the next switch status change. Thus, load R absorbs energy from C_0. The equivalent circuit is shown in Fig. 4(e).

Mode VI [t_5, t_6]: At the beginning of this mode, switch S_1 is turned off, but switch S_2 remains on state, so the voltage across S_2 is zero. The equivalent circuit diagram is shown in Fig. 4(f). Diodes D_2 and D_4 are turned on, the loop of C_5, N_{12} and N_{22} absorbs energy from C_1 and L_{m1}, by the voltage boosted across N_{12} and N_{22}. Capacitor C_2 continues to discharge, leading to D_5 conduction and triggering L_{m1} and C_3 to transfer energy to C_4 via D_5. When C_4 is stable, D_5 is turned off after the current reaches zero. At this time, the energy of load R is provided by C_0.

Due to the presence of parasitic capacitance, the currents of inductors L_{m1} and L_{k1} charge switch S_1, and the coupled current affects the currents of diodes D_2 and D_4.

$$V_{\mathrm{S1}}(t)=\frac{i_{\mathrm{Lm1}}(t)}{C_{\mathrm{S1\_self}}}(t-t_3) \tag{5}$$

$$i_{\mathrm{D2}}(t)+i_{\mathrm{D4}}(t)=\frac{1}{n}\left(i_{\mathrm{Lm1}}(t)-i_{\mathrm{Lk1}}(t)\right) \tag{6}$$

III. STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

This section presents the steady-state analysis of the proposed converter. It is assumed that the magnetizing inductors (L_{m1} and L_{m2}) have the same value, as well as the leakage inductors (L_{k1} and L_{k2}). This relationship is defined by the coupling coefficients of the two coupled inductors as follows:

$$\begin{cases} k_1=\dfrac{L_{\mathrm{m1}}}{L_{\mathrm{m1}}+L_{\mathrm{k1}}} \\ k_2=\dfrac{L_{\mathrm{m2}}}{L_{\mathrm{m2}}+L_{\mathrm{k2}}} \end{cases} \tag{7}$$

A. Voltage Gain

While switch S_1 is on, the voltage across the magnetizing inductors (L_{m1} and L_{m2}) and leakage inductors (L_{k1} and L_{k2}) can be presented as:

$$\begin{cases} V_{\mathrm{Lm1\_on}}=k_1V_{\mathrm{g}} \\ V_{\mathrm{Lk1\_on}}=(1-k_1)V_{\mathrm{g}} \end{cases} \tag{8}$$

According to the volt-second balance law of inductance, when switch S_1 is turned off, the voltages across the inductors (L_{m1} and L_{k1}) are presented as:

$$\begin{cases} V_{\mathrm{Lm1\_off}}=-Dk_1V_{\mathrm{g}}/(1-D) \\ V_{\mathrm{Lk1\_off}}=-D(1-k_1)V_{\mathrm{g}}/(1-D) \end{cases} \tag{9}$$

Similarly, the voltages across magnetizing and leakage inductors (L_{m1} and L_{m2}) can be obtained when switch S_2 is turn on and off, and replace "1" with "2". The negative sign in the formula only indicates direction.

The voltage across the inductor consists of the leakage inductance voltage and the magnetizing inductance voltage. The primary voltage of the transformer can be described as:

$$\begin{cases} V_{\mathrm{N11\_off}}=V_{\mathrm{Lm1}}+V_{\mathrm{Lk1}}=-DV_{\mathrm{g}}/(1-D) \\ V_{\mathrm{N21\_off}}=V_{\mathrm{Lm2}}+V_{\mathrm{Lk2}}=-DV_{\mathrm{g}}/(1-D) \end{cases} \tag{10}$$

According to Kirchhoff voltage law (KVL) in the loops of Fig. 4(c), the following equations can be obtained:

$$\begin{cases} V_{\mathrm{N11\_on}}-V_{\mathrm{g}}=0 \\ V_{\mathrm{N22\_off}}-V_{\mathrm{N12\_on}}-V_{\mathrm{C2}}+V_{\mathrm{C3}}-V_{\mathrm{C1}}+V_{\mathrm{C5}}=0 \\ V_{\mathrm{N21\_off}}+V_{\mathrm{C1}}-V_{\mathrm{N11\_on}}=0 \\ V_{\mathrm{N21\_off}}-V_{\mathrm{C4}}+V_{\mathrm{C0}}-V_{\mathrm{g}}=0 \end{cases} \tag{11}$$

where $V_{\mathrm{N11\_on}}$ and $V_{\mathrm{N12\_on}}$ are the voltages of N_{11} and N_{12} when S_1 is on, while $V_{\mathrm{N21\_off}}$ and $V_{\mathrm{N22\_off}}$ are the voltages of N_{21} and N_{22} when S_2 is off, respectively.

Utilizing KVL in the loops of Fig. 4(f), the following equations can be expressed:

$$\begin{cases} V_{\mathrm{N21\_on}}-V_{\mathrm{g}}=0 \\ V_{\mathrm{N21\_on}}-V_{\mathrm{C4}}+V_{\mathrm{C3}}-V_{\mathrm{N11\_off}}=0 \\ V_{\mathrm{N21\_on}}-V_{\mathrm{N12\_off}}+V_{\mathrm{N22\_on}}-V_{\mathrm{C2}}+V_{\mathrm{C1}}-V_{\mathrm{N11\_off}}=0 \\ V_{\mathrm{N21\_on}}-V_{\mathrm{C5}}-V_{\mathrm{C2}}+V_{\mathrm{C1}}-V_{\mathrm{N11\_off}}=0 \end{cases} \tag{12}$$

where $V_{\mathrm{N11\_on}}$ and $V_{\mathrm{N12\_on}}$ are the voltages of N_{11} and N_{12} when S_1 is off; while $V_{\mathrm{N21\_off}}$ and $V_{\mathrm{N22\_off}}$ are the voltages of N_{21} and N_{22} when S_2 is on, respectively.

The transformer turns ratio n is defined as:

$$\frac{N_{12}}{N_{11}}=\frac{N_{22}}{N_{21}}=n \tag{13}$$

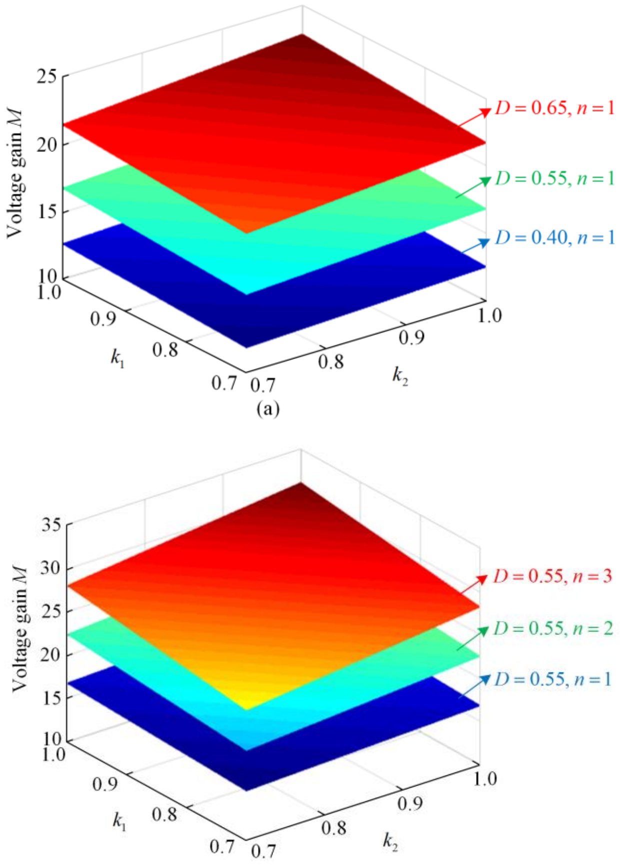
The following relationship can be obtained:

$$\begin{cases} V_{\mathrm{N12\_on}}=n\cdot V_{\mathrm{Lm1\_on}},V_{\mathrm{N12\_off}}=n\cdot V_{\mathrm{Lm1\_off}} \\ V_{\mathrm{N22\_on}}=n\cdot V_{\mathrm{Lm2\_on}},V_{\mathrm{N22\_off}}=n\cdot V_{\mathrm{Lm2\_off}} \end{cases} \tag{14}$$

From (7)–(14), the voltage gain M in the proposed converter can be solved as:

$$M=\frac{[5+(2-D)\cdot n\cdot k_2+(1+D)\cdot n\cdot k_1]}{1-D} \tag{15}$$

Figure 6 is drawn according to (15). Figure 6(a) shows in detail the influence of coupling coefficients k_1 and k_2 on the voltage gain M for different duty cycles D when the turn ratio n is 1. In the same way, Fig. 6(b) shows in detail the impact of coupling coefficients k_1 and k_2 on the voltage gain M for different turns ratios n when the duty cycle D is 0.55. The results show that increasing k_1 or k_2 increases the voltage gain M.



(a)

(b)

Fig. 6. Voltage gain versus leakage inductors for various duty cycles and turns ratios.

Assuming n is 1, Fig. 7 is plotted based on (15). In the vicinity of the duty cycle $D=0.5$, k_1 and k_2 influence the voltage gain to the same extent. When the duty cycle $D<0.5$, the influence weight of k_2 increases, whereas when the duty cycle $D>0.5$, the influence weight of k_1 gradually dominates. The duty cycle D used in this experiment is 0.55, so the influence of k_1 on voltage gain in the experiment is greater than that of k_2, but the difference is not significant.

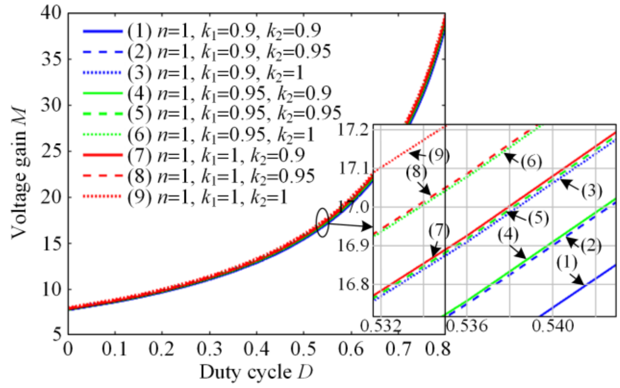


Fig. 7. Relationship between voltage gain and coupling coefficient when n = 1.

Based on the analytical arguments above, we can optimize the process so that the leakage inductance does not exceed 2% of the magnetizing inductance. Therefore, $k=1$ and $k_1=k_2$ can be assumed during the subsequent steady-state analysis process.

$$M=\frac{V_0}{V_g}=\frac{3n+5}{1-D} \tag{16}$$

The voltage gain M versus duty cycle D with different turns ratios n is plotted in Fig. 8.

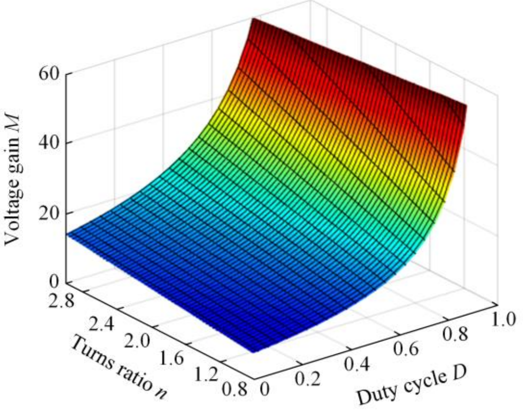


Fig. 8. Voltage gain M versus duty cycle D and turns ratio n.

B. Voltage and Current Stress

The voltage stresses of the diodes, capacitors, and switches are further solved according to Figs. 4(c) and (f), as given in Table I.

TABLE I
VOLTAGE STRESS OF COMPONENTS

Component	Voltage stress	Component	Voltage stress
Switches S_1 and S_2	$\frac{V_0}{3n+5}$	Capacitor C_1	$\frac{V_0}{3n+5}$
Diode D_1, D_5	$\frac{2V_0}{3n+5}$	Capacitor C_2	$\frac{(n+2)V_0}{3n+5}$
Diode D_2, D_3	$\frac{2(n+1)V_0}{3n+5}$	Capacitor C_3	$\frac{3(n+1)V_0}{3n+5}$
Diode D_4	$\frac{2nV_0}{3n+5}$	Capacitor C_4	$\frac{(3n+4)V_0}{3n+5}$
Diode D_0	$\frac{V_0}{3n+5}$	Capacitor C_5	$\frac{nV_0}{3n+5}$

Assuming that there are no loss in the circuit, there is:

$$V_g I_g=V_0 I_0 \Rightarrow I_g=MI_0 \tag{17}$$

Due to the symmetrical structure of the coupled inductor, in steady-state analysis, it can be deduced that:

$$I_{\mathrm{Lm1}}=I_{\mathrm{Lm2}}=\frac{I_g}{2} \tag{18}$$

The time interval between Mode I-II and Mode IV–V is:

$$\Delta t=t_1-t_0=t_3-t_2=\frac{2D-1}{2}T \tag{19}$$

The maximum current through switches S_1 and S_2 is equal to the maximum current through the magnetizing inductors. Kirchhoff's current law (KCL) is applied at the connection point of inductors, capacitors, and diodes. The maximum current is calculated by mode III and mode VI as follows:

$$\left|i_{\mathrm{C}0,1,2,3,4,5}\right| = \left|i_{\mathrm{D}0,1,2,3,4,5}\right| = \frac{I_0}{(1-D)} \tag{20}$$

$$i_{\mathrm{C0\text{-}III}} = \frac{D}{1-D} I_0 \tag{21}$$

where $i_{\mathrm{C0\text{-}III}}$ is the current stress of C_0 in state III.

C. Performance Comparison

Numerous scholars have conducted extensive researches on high step-up converters and proposed various topology structures. To evaluate the performance and parameters of these proposed topologies, comparisons among the topologies are made in the referenced papers. A comparison between the proposed topology and the topologies presented in [15]–[22] is shown in Table II.

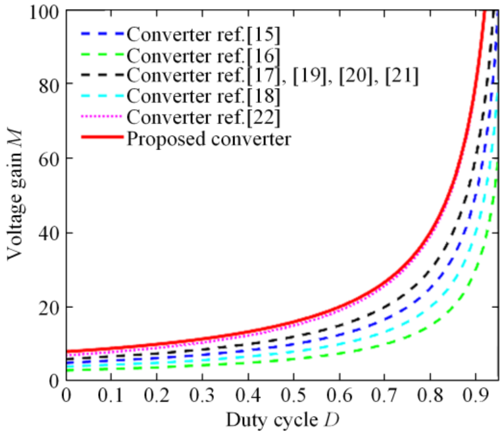
TABLE II
COMPARISON BETWEEN THE PROPOSED CONVERTER AND OTHER CONVERTERS

Converters	Ref. [15]	Ref. [16]	Ref. [17]	Ref. [18]	Ref. [19]	Ref. [20]	Ref. [21]	Ref. [22]	Proposed
Voltage gain	$\frac{2n+3}{1-D}$	$\frac{n+2}{1-D}$	$\frac{2n+4}{1-D}$	$\frac{3n+1}{1-D}$	$\frac{2n+4}{1-D}$	$\frac{2n+4}{1-D}$	$\frac{2n+4}{1-D}$	$\frac{3+4n+D}{1-D}$	$\frac{3n+5}{1-D}$
S/D/W/C	1/5/3/5	2/4/3/3	2/6/4/6	2/5/4/4	2/6/4/6	2/6/4/6	2/4/4/4	2/6/6/8	2/6/4/6
Ground	No	Yes	No	Yes	No	No	Yes	No	Yes
Diode voltage stress	$\frac{(2n+1)V_0}{2n+3}$	V_0	$\frac{nV_0}{n+2}$	$\frac{2nV_0}{3n+1}$	$\frac{nV_0}{n+2}$	$\frac{nV_0}{n+2}$	$\frac{(n+1)V_0}{n+2}$	$\frac{(2n+1)V_0}{3+4n+D}$	$\frac{2(n+1)V_0}{3n+5}$
Switch voltage stress	$\frac{V_0}{2n+3}$	$\frac{V_0}{n+2}$	$\frac{V_0}{2n+4}$	$\frac{V_0}{3n+1}$	$\frac{V_0}{4n+2}$	$\frac{V_0}{2n+4}$	$\frac{V_0}{2n+4}$	$\frac{V_0}{3+4n+D}$	$\frac{V_0}{3n+5}$
Efficiency (%)		94.65	94.65	97.0	95.2	95.8	94.55	97.38	96.25
Power (kW)		3.5	500	400	280	200	300	250	300
Input voltage (V)	25	48	24	40	28	30	40	28	22.6
Output voltage (V)	400	380	400	400	400	400	600	460	400
Frequency (kHz)	40	50	50	50	100	40	40	100	50

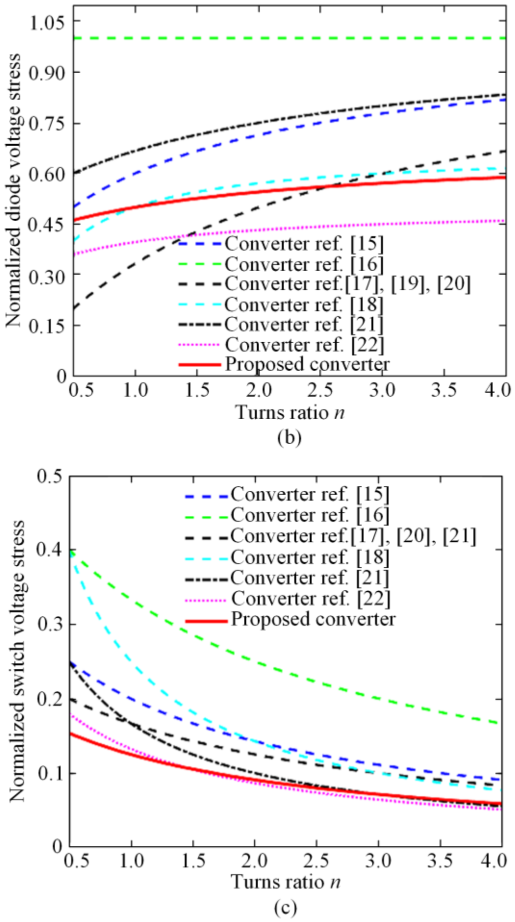
Notes: S represents switch, D is diode, W is winding, and C is capacitor.

Reference [15] proposes a novel DC-DC converter structure consisting of two hybrid multi-voltage units, one switch, and a three-winding coupled inductor. However, increasing the voltage gain of this converter appears to be challenging. Interleaved boost converters with two switches have been extensively studied, as shown in [16]–[22]. Reference [16] proposes this type of circuit. Although fewer devices are used, the voltage stress across them is generally higher. In addition, the ability of the inductance cannot be fully utilized, and the voltage gain of this circuit does not have a significant competitive advantage. References [17]–[21] adopt active clamp techniques, resulting in higher voltage gain and lower voltage stress in the circuits. Reference [22] proposes a converter with a higher voltage gain formula by integrating two high step-up DC-DC converters and more windings. This paper proposes a circuit structure with higher voltage gain without increasing the number of devices and windings. The experimental efficiencies of relevant references are summarized, and the tested efficiency of this prototype under full load conditions is still very competitive, only lower than [18] and [22]. This topology has clear advantages in terms of gain effect compared to [18], whereas [22] is more suitable for light loads, but requires more devices and higher control accuracy requirements.

Table II shows that the voltage gain curves can be drawn when the turns ratio is 1, as demonstrated in Fig. 9. By combining Table II with Fig. 9, it is evident that the proposed converter has fewer devices than those in [17], [19], [20], and [22], while also achieving a higher voltage gain. Furthermore, the proposed converter offers the advantage of a common ground for the input and output voltages. Although the proposed converter requires one or two more capacitors and diodes compared to [19], [20], and [21], its efficiency is slightly improved while its boosting capability is greatly enhanced.



(a)



(b)

(c)

Fig. 9. The performance of the proposed converter is compared with the converters in [15]–[22]. (a) Voltage gain M with n=1. (b) Normalized diode voltage stress. (c) Normalized switch voltage stress.

IV. DESIGN GUIDELINES OF THE PROPOSED CONVERTER

A. Magnetizing Inductor

The voltage gain of this proposed topology can be adjusted by changing the turns ratio of the coupled inductors. To ensure proper operation, the calculated turns ratio n should be less than 3 in the dominant region of the topology. Once the required voltage gain M and duty cycle D are specified, the turns ratio n can be obtained, as:

$$n = \frac{1}{3}\left[M(1-D)-5\right] \tag{22}$$

To ensure the magnetizing inductor works in CCM, the following constraint can be derived:

$$\Delta I_{\mathrm{Lm}} \leqslant 2 I_{\mathrm{Lm}} \tag{23}$$

The current ripple of the magnetizing inductance is:

$$\Delta I_{\mathrm{Lm}} = \frac{V_{\mathrm{g}} D T}{L_{\mathrm{m}}} \tag{24}$$

Using (19), (25), and (26), the range of the magnetizing inductance can be derived as:

$$L_{\mathrm{m}} \geqslant \frac{RD}{2 f_{\mathrm{S}} M^2} \tag{25}$$

where R is the output resistor; T is the switching period; and f_{S} is the switching frequency.

Ferrite core material is the primary material used for making such inductors. According to [26], the A_{P} value can be obtained as:

$$A_{\mathrm{P}} = A_{\mathrm{e}} A_{\mathrm{w}} = \frac{(P_0/\eta + P_0)}{2\Delta B f_{\mathrm{S}} J k_{\mathrm{u}}} \tag{26}$$

where ΔB, P_0, J and k_{u} are the flux density swing, output power, ampere density, and copper window coefficient, respectively, which are assumed to be 0.4 T, 300 W, 200 A/cm^2, and 0.2, respectively; η is the transformation efficiency assumed to be 95%. By calculation, the A_{P} value is 3.85 cm^4. By looking up Table III, the model EE42 is selected, and its A_{P} value is 4.9484 cm^4.

Table III
MAGNETIC CORE PARAMETERS

Type	Material ferrite	A_{p} (cm^4)	A_{e} (mm^2)	A_{w} (mm^2)
EE4133	PC40	2.8260	157.00	180.00
EE42/21/15	PC40	4.9484	178.00	278.00
EE47/39	PC40	4.7529	242.00	196.40
EE50	PC40	5.7343	226.00	253.73

The turns of N_{11} and N_{21} can be calculated using the following formula:

$$N = \frac{V T_{\mathrm{on}}}{A_e \Delta B} = \frac{V_{\mathrm{g}} D}{f_{\mathrm{S}} A_e \Delta B} \tag{27}$$

In order to facilitate the opening of the air gap, the number of turns is determined to be more than 7. The core air gap is calculated as follows:

$$A_{\mathrm{g}} = \frac{0.001256 A_{\mathrm{e}} N^2}{L_{\mathrm{m}}} \tag{28}$$

The diameter of the copper wire can be calculated from:

$$d_{\mathrm{wp}} = 1.13\sqrt{I_{\mathrm{Lk\_RMS}}/J} = 2.06\ \mathrm{mm} \tag{29}$$

The current skin depth is:

$$d_{\mathrm{wH}} = \frac{137.7}{\sqrt{f_{\mathrm{S}}}} = 0.62\ \mathrm{mm} \tag{30}$$

In the proposed converter, 3 strands of 1.0 mm enameled wire are used, which can meet the requirements.

Table I can be used to determine the appropriate switches and diodes. It should be noted that voltage spikes can occur during switching transitions in these devices, both in the on and off states. Therefore, the selected devices should have a withstand voltage value that is 50% higher than the calculated value.

B. Capacitor

The key parameter for designing the capacitors is the acceptable voltage ripple value (r %), which can be selected based on the output current I_0, switching frequency f_{S}, duty cycle D, turns ratio of the coupled inductor n, and input voltage. The capacitance range of the required capacitors can be calculated from:

$$C_i \geqslant \frac{|i_{\mathrm{C}i}|(1-D)}{r\% V_{\mathrm{C}i} f_{\mathrm{S}}},\ (i=0,1,2,3,4,5) \tag{31}$$

where r is the capacitor voltage ripple rate.

C. Theoretical Loss of the Proposed Converter

In this subsection, the calculation of the losses of the devices is presented. The power losses of the proposed prototype include the power dissipation of the switches, diodes, coupled inductors, and capacitors. Table IV lists the parasitic parameters of all devices, and Fig. 10 shows the equivalent circuit with these parameters. The switching process in a semiconductor device causes a change in the input voltage, and the change in the charge of the input capacitor affects the internal charge distribution of the device. This effect is known as the Miller effect. As shown in Fig. 11, the Miller effect has a significant impact on the performance of a switching device by increasing the equivalent input and output capacitance of the switch and decreasing the bandwidth and speed. In addition, the Miller effect increases the input current of the switch, which leads to increased power consumption and heat dissipation. Therefore, it is important to consider the Miller effect in the calculation of switching losses.

TABLE IV
DRIVE AND COMPONENT PARAMETERS OF THE PROTOTYPE

Symbol	Value	Symbol	Value
MOSFET gate-to-source voltage, V_{GS} (V)	15	Equivalent series resistance of N_{21}, r_{N21} (mΩ)	14.0
MOSFET gate threshold voltage, $V_{\mathrm{GS(th)}}$ (V)	3	Equivalent series resistance of N_{22}, r_{N22} (mΩ)	13.5
MOSFET miller platform voltage, V_{GP} (V)	6.3	Equivalent series resistance of $\mathrm{C}_{2,3,4,0}$, $r_{\mathrm{C2,C3,C4,C0}}$ (mΩ)	12.0
MOSFET drive turn-on resistance, R_{on} (Ω)	10	Equivalent series resistance of $\mathrm{C}_{1,5}$, $r_{\mathrm{C1,C5}}$ (mΩ)	8.0
MOSFET drive turn-off resistance, R_{off} (Ω)	1	Threshold voltage of $\mathrm{D}_{0,1,5}$, $V_{\mathrm{FD0,1,5}}$ (V)	0.75
MOSFET drive internal resistance, R_{G} (Ω)	1	Threshold voltage of $\mathrm{D}_{2,3,4}$, $V_{\mathrm{FD2,3,4}}$ (V)	1.07
MOSFET input capacitance, G_{ISS} (pF)	10 720	Forward resistance of $\mathrm{D}_{0,1,5}$, $r_{\mathrm{D0,1,5}}$ (Ω)	0.008
MOSFET gate-to-drain (miller) charge, Q_{GD} (nC)	52	Forward resistance of $\mathrm{D}_{2,3,4}$, $r_{\mathrm{D2,3,4}}$ (Ω)	0.006
MOSFET static drain-to-source on-resistance, $r_{\mathrm{DS1,2}}$ (Ω)	0.008	Reverse recovery current of reverse diode $\mathrm{D}_{0,1,5}$, $I_{\mathrm{rrD0,1,5}}$ (A)	0.25
Forward voltage of reverse diode, V_{SD} (V)	0.9	Reverse recovery current of reverse diode $\mathrm{D}_{2,3,4}$, $I_{\mathrm{rrD2,3,4}}$ (A)	0.25
Equivalent series resistance of N_{11}, r_{N11} (mΩ)	13.9	Reverse recovery time of reverse diode $\mathrm{D}_{0,1,5}$, $t_{\mathrm{rrD0,1,5}}$ (s)	55×10^{-9}
Equivalent series resistance of N_{12}, r_{N12} (mΩ)	13.9	Reverse recovery time of reverse diode $\mathrm{D}_{2,3,4}$, $t_{\mathrm{rrD2,3,4}}$ (s)	60×10^{-9}

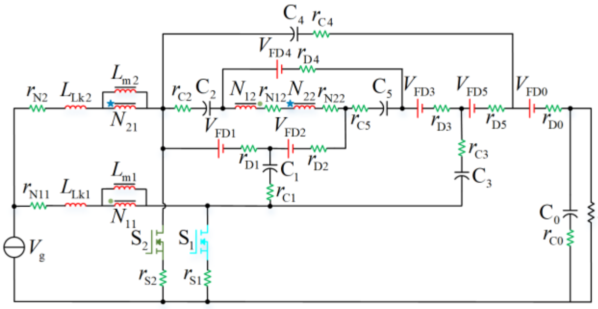


Fig. 10. The equivalent circuit of the converter takes into account parasitic parameters.

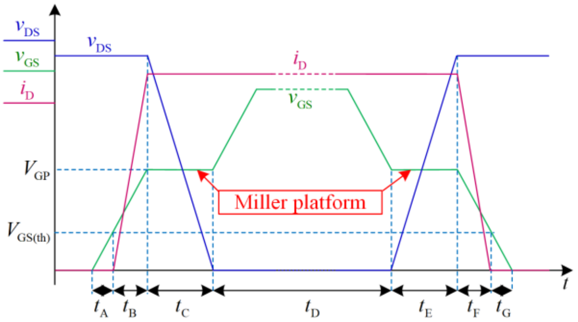


Fig. 11. Detailed process of the Miller platform.

As shown in Fig. 11, V_{GS} is the output voltage of the PWM gate driver. The time t_{B} for the V_{GS} voltage to increase from $V_{\mathrm{GS(th)}}$ to the Miller platform voltage V_{GP} is presented in (32). In the same way, t_{F} is the time for V_{GS} to decrease from the Miller platform voltage V_{GP} to $V_{\mathrm{GP(th)}}$, as shown in (33).

$$\begin{aligned} t_{\mathrm{B}} &= (R_{\mathrm{G}}+R_{\mathrm{on}})\cdot C_{\mathrm{ISS}}\cdot\left[\ln\frac{1}{1-\frac{V_{\mathrm{GP}}}{V_{\mathrm{GS}}}}-\ln\frac{1}{1-\frac{V_{\mathrm{GS(th)}}}{V_{\mathrm{GS}}}}\right]= \\ &(R_{\mathrm{G}}+R_{\mathrm{on}})\cdot C_{\mathrm{ISS}}\cdot\left[\ln\left(\frac{V_{\mathrm{GS}}-V_{\mathrm{GS(th)}}}{V_{\mathrm{GS}}-V_{\mathrm{GP}}}\right)\right]=37.92\text{ ns} \end{aligned} \tag{32}$$

$$\begin{aligned} t_{\mathrm{F}} &= (R_{\mathrm{G}}+R_{\mathrm{off}})\cdot C_{\mathrm{ISS}}\cdot\left[\ln\frac{1}{1-\frac{V_{\mathrm{GP}}}{V_{\mathrm{GS}}}}-\ln\frac{1}{1-\frac{V_{\mathrm{GS(th)}}}{V_{\mathrm{GS}}}}\right]= \\ &(R_{\mathrm{G}}+R_{\mathrm{off}})\cdot C_{\mathrm{ISS}}\cdot\left[\ln\left(\frac{V_{\mathrm{GS}}-V_{\mathrm{GS(th)}}}{V_{\mathrm{GS}}-V_{\mathrm{GP}}}\right)\right]=9.31\text{ ns} \end{aligned} \tag{33}$$

The calculation of the maintenance time t_{C} and t_{E} is given as:

$$t_{\mathrm{C}}=Q_{\mathrm{GD}}\cdot\frac{R_{\mathrm{G}}+R_{\mathrm{on}}}{V_{\mathrm{GS}}-V_{\mathrm{GP}}}=65.75\ \mathrm{ns}\tag{34}$$

$$t_{\mathrm{E}}=Q_{\mathrm{GD}}\cdot\frac{R_{\mathrm{G}}+R_{\mathrm{off}}}{V_{\mathrm{GS}}-V_{\mathrm{GP}}}=16.14\ \mathrm{ns}\tag{35}$$

The switch power loss includes conduction loss and switching loss. The switching loss of single switch is expressed as:

$$\begin{aligned}P_{\mathrm{sw\_S}i}&=\frac{1}{T}\left(\begin{array}{l}\int_0^{t_{\mathrm{r}}}V_{\mathrm{S}i}i_{\mathrm{S}i\mathrm{r}}\mathrm{d}t+\int_0^{t_{\mathrm{f}}}V_{\mathrm{S}i}i_{\mathrm{S}i\mathrm{f}}\mathrm{d}t)=\\ \frac{1}{2}f_{\mathrm{S}}V_{\mathrm{S}i}(i_{\mathrm{S}i\mathrm{r}}t_{\mathrm{r}}+i_{\mathrm{S}i\mathrm{f}}t_{\mathrm{f}}\end{array}\right)=\\&\frac{1}{2}f_{\mathrm{S}}V_{\mathrm{S}i}[i_{\mathrm{S}i\mathrm{r}}(t_{\mathrm{B}}+t_{\mathrm{C}})+i_{\mathrm{S}i\mathrm{f}}(t_{\mathrm{F}}+t_{\mathrm{E}})]\end{aligned}\tag{36}$$

where $i_{\mathrm{S}i\mathrm{r}}$ and $i_{\mathrm{S}i\mathrm{f}}$ are the switch rise and fall currents, respectively, and their values are the currents in mode I, II, IV and V, respectively; t_{r} and t_{f} are the rise and fall times of the switch.

The conduction loss of the switches is:

$$P_{\mathrm{cond\_S}i}=\frac{1}{T}\int_0^T r_{\mathrm{S}}i_{\mathrm{S}}^2\mathrm{d}t\ =r_{\mathrm{S}}I_{\mathrm{S\_RMS}}^2\tag{37}$$

where $I_{\mathrm{S\_RMS}}$ is the current RMS value flowing through the switch.

Therefore, the total switch power loss for the two switches is given as:

$$\begin{aligned}P_{\mathrm{S\_loss}}=&\sum(P_{\mathrm{cond\_S}i}+P_{\mathrm{sw\_S}i}),\ (i=1,2)=\\&\frac{f_{\mathrm{S}}\cdot V_0}{3n+5}\frac{M\cdot I_0}{2}[t_{\mathrm{B}}+t_{\mathrm{C}}+t_{\mathrm{F}}+t_{\mathrm{E}}]+\\&r_{\mathrm{DS1}}\left((2D-1)\left(\frac{M\cdot I_0}{2}\right)^2+(1-D)\left(I_0M-\frac{I_0}{1-D}\right)^2\right)+\\&r_{\mathrm{DS2}}\left((2D-1)\left(\frac{M\cdot I_0}{2}\right)^2+(1-D)\left(\frac{M\cdot I_0}{2}\right)^2\right)\end{aligned}\tag{38}$$

Diode power loss includes conduction loss and switching loss. Diode conduction loss is:

$$\begin{aligned}P_{\mathrm{cond\_D}i}&=\frac{1}{T}\int_0^T(V_{\mathrm{FD}i}i_{\mathrm{D}i}+r_{\mathrm{D}i}i_{\mathrm{D}i}^2)\mathrm{d}t=\\&V_{\mathrm{FD}i}I_{\mathrm{D}i\mathrm{\_ave}}+r_{\mathrm{D}i}I_{\mathrm{D}i\mathrm{\_RMS}}^2,\ (i=0,1,2,3,4,5)\end{aligned}\tag{39}$$

where $V_{\mathrm{FD}i}$ is the forward voltage drop; $I_{\mathrm{D}i\mathrm{\_ave}}$ and $I_{\mathrm{D}i\mathrm{\_RMS}}$ represent the current average and RMS value flowing through diode D_i.

Diode switching loss can be calculated as:

$$\begin{aligned}P_{\mathrm{sw\_D}i}&=\frac{1}{T}\int_0^{t_{\mathrm{rrD}i}}P_{\mathrm{D}i}(t)\mathrm{d}t=\\&\frac{1}{2}f_{\mathrm{S}}V_{\mathrm{D}i}I_{\mathrm{rrD}i}t_{\mathrm{rrD}i},\ (i=0,1,2,3,4,5)\end{aligned}\tag{40}$$

where $V_{\mathrm{D}i}$ is the voltage stress of the diode; $I_{\mathrm{rrD}i}$ is the reverse recovery current; $t_{\mathrm{rrD}i}$ is the reverse recovery time.

There are six diodes in this topology, and the total diode loss can be derived as:

$$\begin{aligned}P_{\mathrm{D\_loss}}=&\sum(P_{\mathrm{cond\_D}i}+P_{\mathrm{sw\_D}i}),\ \ (i=0,1,2,3,4,5)=\\&3(1-D)\left(V_{\mathrm{FD0,1,5}}\frac{I_0}{1-D}+r_{\mathrm{D0,1,5}}\left(\frac{I_0}{1-D}\right)^2\right)+\\&3(1-D)\left(V_{\mathrm{FD2,3,4}}\frac{I_0}{1-D}+r_{\mathrm{D2,3,4}}\left(\frac{I_0}{1-D}\right)^2\right)+\\&\frac{1}{2}f_{\mathrm{S}}I_{\mathrm{rrD0,1,5}}\cdot t_{\mathrm{rrD0,1,5}}\cdot\frac{5V_0}{5+3n}+\\&\frac{1}{2}f_{\mathrm{S}}I_{\mathrm{rrD2,3,4}}\cdot t_{\mathrm{rrD2,3,4}}\cdot\frac{(4+6n)V_0}{5+3n}\end{aligned}\tag{41}$$

The loss of capacitor can be determined as:

$$\begin{aligned}P_{\mathrm{cond\_C}i}&=\frac{1}{T}\left(\int_0^{DT}r_{\mathrm{C}i}i_{\mathrm{C}i\mathrm{\_on}}^2\mathrm{d}t+\int_{DT}^T r_{\mathrm{C}i}i_{\mathrm{C}i\mathrm{\_off}}^2\mathrm{d}t\right)=\\&r_{\mathrm{C}i}I_{\mathrm{C}i\mathrm{\_RMS}}^2,\ (i=0,1,2,3,4,5)\end{aligned}\tag{42}$$

where $I_{\mathrm{C}i\mathrm{\_RMS}}$ is the current RMS value flowing through capacitor C_i.

The total power loss of capacitors is obtained as:

$$\begin{aligned}P_{\mathrm{C\_loss}}=&\sum r_{\mathrm{C}i}I_{\mathrm{C}i\mathrm{\_RMS}}^2,\ (i=0,1,2,3,4,5)=\\&2\cdot 2r_{\mathrm{C1,5}}(1-D)\left(\frac{I_0}{1-D}\right)^2+3\cdot 2r_{\mathrm{C2,3,4}}(1-D)\left(\frac{I_0}{1-D}\right)^2+\\&r_{\mathrm{C0}}(1-D)\left(\frac{DI_0}{1-D}\right)^2+r_{\mathrm{C0}}(1-D)\left(\frac{I_0}{1-D}\right)^2\end{aligned}\tag{43}$$

Losses related to high-frequency transformers and inductors are categorized as conduction losses and core losses. The conduction loss of the coupled inductors can be obtained as follows:

$$\begin{aligned}P_{\mathrm{CI\_cond}}=&\sum_{i=1,\,j=1}^{2}r_{\mathrm{N}ij}I_{\mathrm{N}ij\mathrm{\_RMS}}^2,\ (i=1,2;\ j=1,2)=\\&r_{\mathrm{N11}}I_{\mathrm{Lk1\_RMS}}^2+r_{\mathrm{N12}}I_{\mathrm{N12\_RMS}}^2+\\&r_{\mathrm{N21}}I_{\mathrm{Lk2\_RMS}}^2+r_{\mathrm{N22}}I_{\mathrm{N22\_RMS}}^2\end{aligned}\tag{44}$$

The hysteresis loss and the eddy current loss of the ferrite core are given by the Steinmetz equation in [27], as:

$$P_{\mathrm{core}}=P_{\mathrm{V}}V=FKf_{\mathrm{S}}^{\alpha}B^{\beta}V\tag{45}$$

where P_{V} is the core loss power density; V is the core effective volume in the transformer; F is the flux waveform factor with a value of $\pi/4$, B is the flux density in the core; K, α and β are constants, for ferrite core materials, the values are 4.88×10^{-5}, 1.63 and 6.22, respectively.

In [28], the core flux density can be expressed by:

$$B=\frac{V_{\mathrm{N\_on}}D}{4NA_ef_{\mathrm{S}}}\tag{46}$$

where $V_{\mathrm{N\_on}}$ is the voltage across the inductor when the switch turns on, and N is the number of turns.

Then, the loss of inductance can be summarized as:

$$P_{\text{CI\_loss}} = P_{\text{CI\_cond}} + P_{\text{core1}} + P_{\text{core2}} \tag{47}$$

There are two coupled inductors in this converter with four windings and six capacitors. The total losses of the proposed converter are expressed as:

$$P_{\text{loss}} = P_{\text{S\_loss}} + P_{\text{D\_loss}} + P_{\text{CI\_loss}} + P_{\text{C\_loss}} \tag{48}$$

Thus, the conversion efficiency is calculated as:

$$\eta = \frac{P_0}{P_0 + P_{\text{loss}}} \times 100\% \tag{49}$$

The parameters of the converter in the experiment are summarized in Table IV and Table V, and substituted into (32)–(48). The relationship between the efficiency and the output power is shown in Fig. 12. In the low power stage, the efficiency increases rapidly with the output power. When the duty cycle is 0.55 and the converter output power is 100 W, the efficiency reaches a maximum value of 97.27%. As the power increases, the losses also increase. When the output power is 300 W, the theoretical efficiency is 96.94%. Similarly, under different duty cycles and gain conditions, the trend of the theoretical efficiency curve remains the same. The theoretical efficiency values are above 95% within a wide range of duty cycles. Therefore, the proposed converter has the advantage of high efficiency.

TABLE V
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameter	Value	Parameter	Value
Input voltage (V)	20–48	Rated power (W)	300
Output voltage (V)	400	L_{k1} , L_{k2} (μH)	<1.30
L_{m1} , L_{m2} (μH)	130	n	1
MOSFETs	IRFP4668PbF	C_1 , C_5 (μH)	10
D_0 , D_1 , D_5	STTH6003CW	C_2 , C_3 , C_4 , C_0 (μH)	5.6
D_2 , D_3 , D_4	STTH6006	Switch frequency (kHz)	50

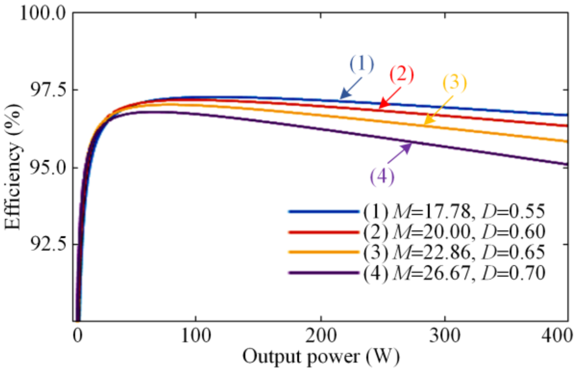


Fig. 12. Theoretical efficiency versus power output.

Figure 13 displays the temperature distribution of the proposed converter when operating at an output power of 300 W. A thermal imager (FLUKE Ti400) is used for the measurements. The prototype is operated at an ambient temperature of 23.8 °C, the maximum temperature measured on switching devices is 41.3 °C, as indicated by the dark red color block; while the minimum temperature at the edge of the PCB board and the desk is 22.1°C, as indicated by the dark black color block. The temperature distribution shows that the switches have the highest temperature, followed by the diode and the core, while the capacitors have the lowest temperature, which is in accordance with the loss calculations.

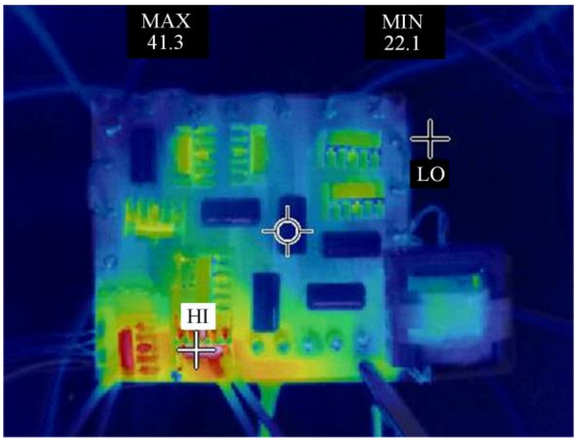


Fig. 13. The temperature distribution of the proposed converter when $P_0 = 300$ W.

Based on the different output power, the percentage of loss of each type of device is calculated and plotted in Fig. 14. As the output power increases, the percentage of current related loss also increases. It is clear that the percentages of MOSFETs losses, CIs conduction losses and capacitors losses increase gradually with the increase in output power. Upon further analysis of the loss composition at 300 W power and 0.55 duty cycle, it is observed that the dominant power losses are related to diode losses. Details of power losses are provided in Fig. 15, followed by losses in the MOSFETs, windings, capacitors, and cores, accounting for 3.35 W (35.45%), 1.41 W (14.94%), 0.14 W (1.46%), and 0.134 W (1.42%), respectively.

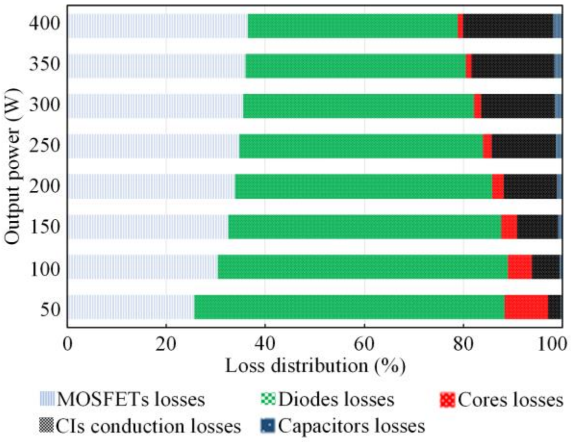


Fig. 14. Various loss ratios for different output powers.

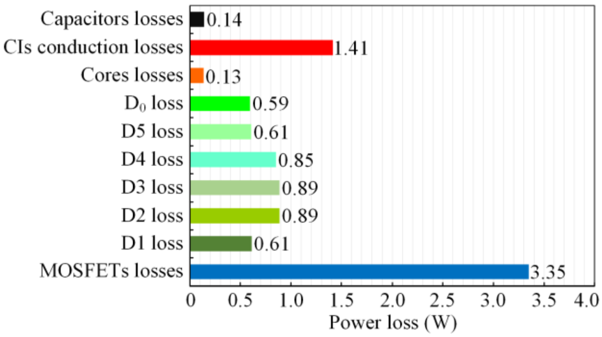


Fig. 15. Loss distribution of the proposed converter when $D = 0.55$ and $P_0 = 300$ W.

V. EXPERIMENTAL VERIFICATION

To evaluate the practicality of the suggested converter, tests are conducted on a laboratory prototype, as illustrated in Fig. 16. Additionally, an experimental platform is shown in Fig. 17. The parameters of the prototype converter are presented in Table V. The PWM gate pulses of the switches are generated by a DSP28335 with an appropriate dead time. The switching frequency and duty cycle are set to 50 kHz and 0.55, respectively. The captured experimental waveforms are illustrated in Figs. 18 and 19.

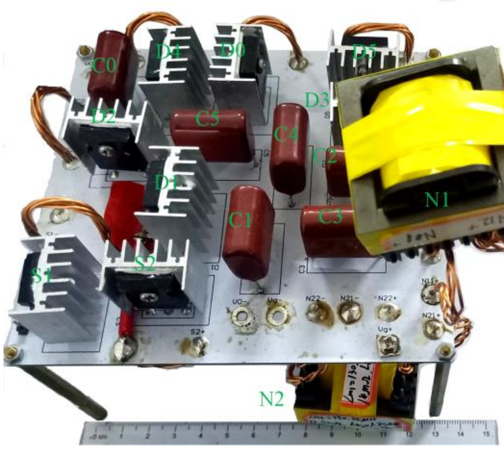


Fig. 16. Implemented proposed converter prototype.

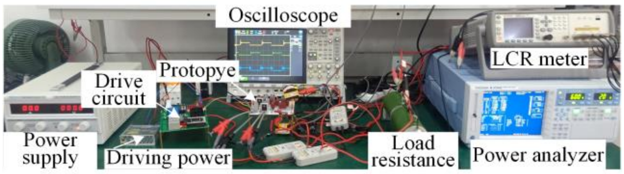
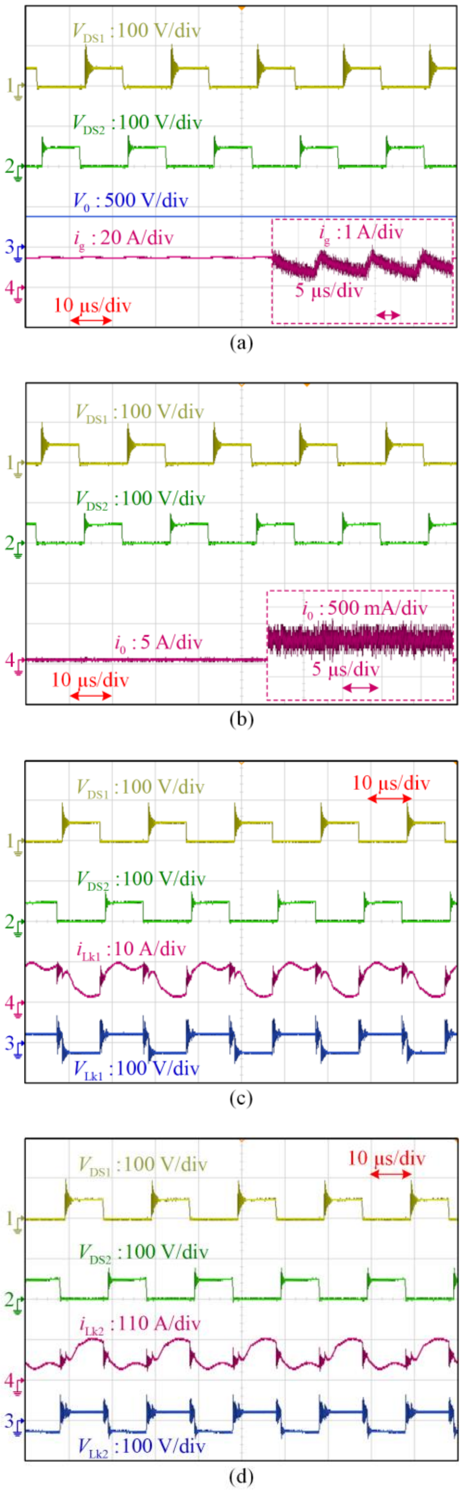
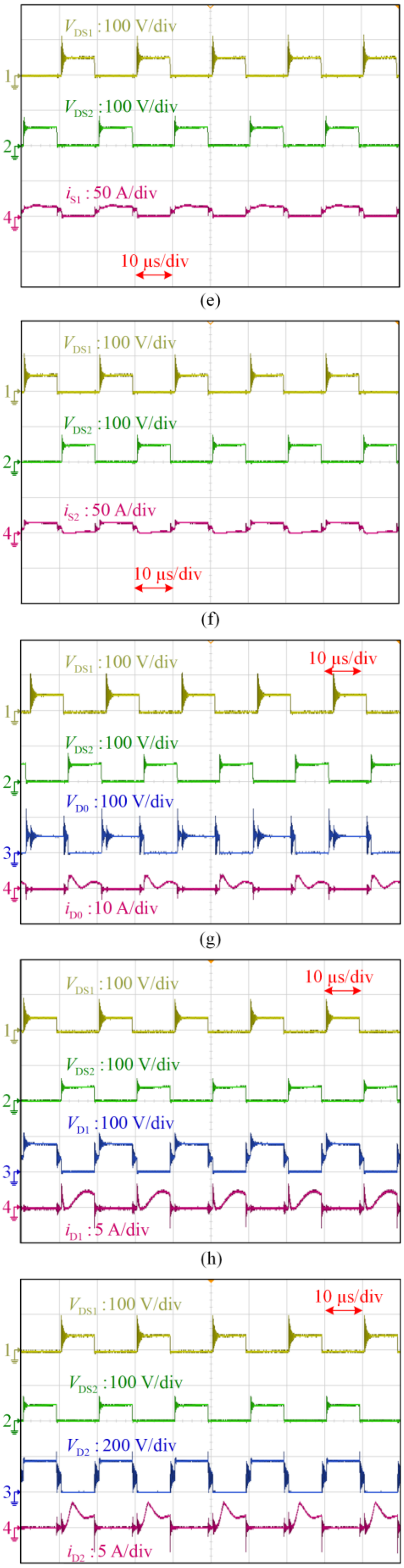


Fig. 17. Laboratory prototype and experimental platform.

The experimental results are measured using a YOKOGAWA WT300E power analyzer. As shown in Figs. 18(a) and (b), at an output power of 300 W, the input voltage is 22.62 V, the average input current is 13.785 A with a ripple of less than 7%. The output current ripple is less than 500 mA. The proposed converter has a voltage gain of 17.64, which is slightly lower than the theoretical value due to the parasitic parameters of the components. The collected data under different output power conditions indicate that the converter is highly efficient, with an output voltage of 398.95 V and an output current of 0.75 A.





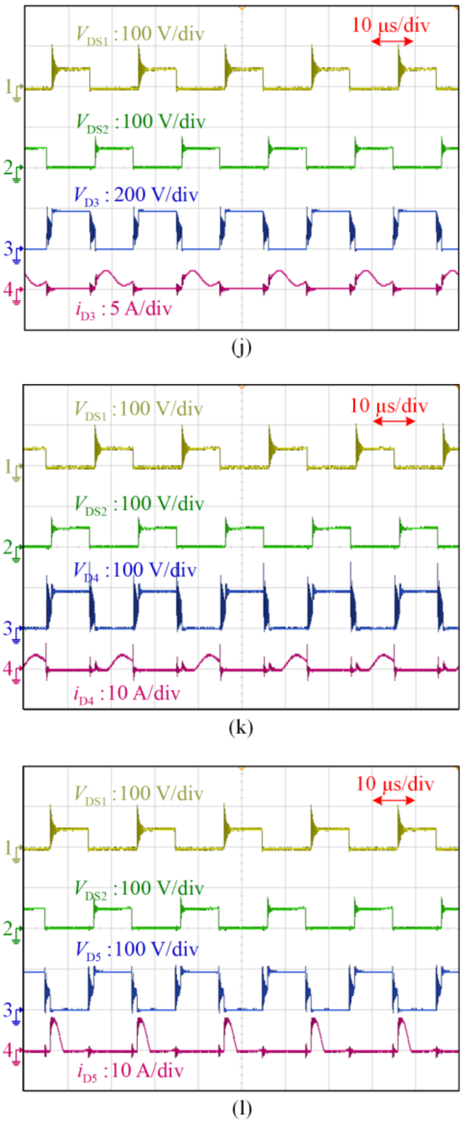
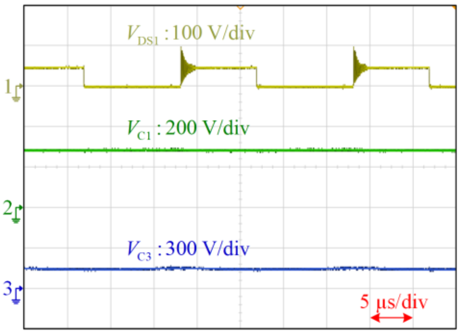
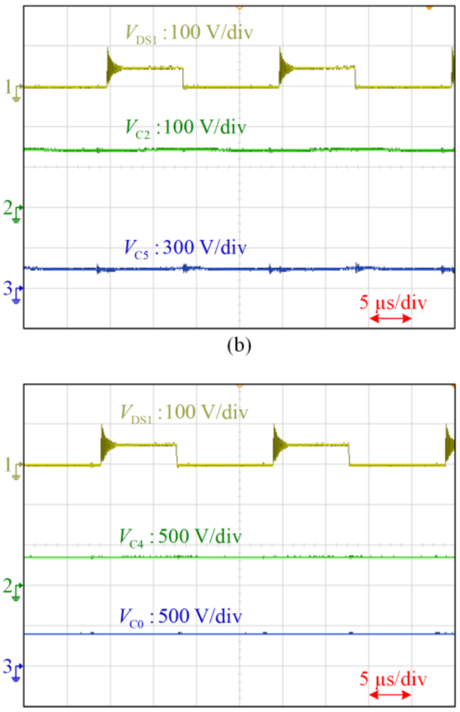


Fig. 18. Experimental waveforms of the proposed converter when $D = 0.55$ and $P_0 = 300$ W. (a) V_{DS1}, V_{DS2}, V_0, i_g. (b) V_{DS1}, V_{DS2}, i_0. (c) V_{DS1}, V_{DS2}, V_{Lk1}, i_{Lk1}. (d) V_{DS1}, V_{DS2}, V_{Lk2}, i_{Lk2}. (e) V_{DS1}, V_{DS2}, i_{S1}. (f) V_{DS1}, V_{DS2}, i_{S2}. (g) V_{DS1}, V_{DS2}, V_{D0}, i_{D0}. (h) V_{DS1}, V_{DS2}, V_{D1}, i_{D1}. (i) V_{DS1}, V_{DS2}, V_{D2}, i_{D2}. (j) V_{DS1}, V_{DS2}, V_{D3}, i_{D3}. (k) V_{DS1}, V_{DS2}, V_{D4}, i_{D4}. (l) V_{DS1}, V_{DS2}, V_{D5}, i_{D5}.



(a)



(b)

(c)

Fig. 19. Experimental results of C_1, C_2, C_3, C_4, C_5, and C_0 in the proposed converter when $D = 0.55$ and $P_0 = 300$ W.

From Figs. 18(c) and (d), it can be observed that i_{Lk2} phase lags i_{Lk1} by 180°, which is a characteristic of the interleaved converter for reducing the input current ripple. Figs. 18(e) and (f) show the voltage and current waveforms of switches S_1 and S_2. According to Table I, the voltage stress should be approximately 50 V. The diode on/off states in Figs. 18(g)–(l) are consistent with the theoretical analysis and the voltage stresses are less than 50 V, 100 V, 200 V, 200 V, 100 V, and 100 V, respectively, which are in line with the theoretical calculation according to Table I.

The voltage waveforms of capacitors $C_0 - C_5$ shown in Fig. 19 are also consistent with the calculation results from Table I. The experimental results demonstrate that the prototype satisfies the design requirements and the topology is stable.

Figure 20 shows the measured efficiencies at different output power. A noticeable difference exists between the theoretical and measured efficiencies at different output power when the output voltage remains stable at 400 V. The differences between the measured and theoretical efficiencies are caused by parasitic parameters resulting from tolerances in PCB manufacturing and measurement equipment. It can be observed that the efficiency of the converter decreases with a small slope as the output power increases. The main reason is that as the power increases, the current increases, leading to increased losses associated with the current and therefore decreased efficiency.

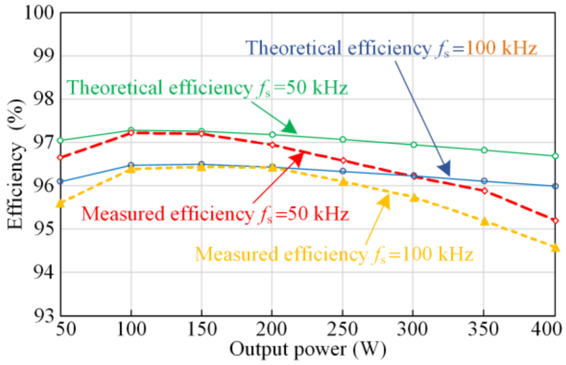


Fig. 20. Experimental efficiency curve of the proposed converter.

The experimental results show that the efficiency reaches more than 97% at the output power of 100 W, which is the highest efficiency power point. At a switching frequency of 50 kHz and a rated output power of 300 W, the efficiency of the proposed prototype is 96.25%. This efficiency is 0.69% lower than the theoretical value due to line heating and equipment errors, but is consistent with the actual situation. The same is true for a switching frequency of 100 kHz. The increase in switching frequency mainly leads to an increase in the switch and diode switching losses, while the losses related to current conduction remain unchanged, thus maintaining a high operating efficiency. It is clear that the proposed prototype has excellent performance and is valuable for commercial applications.

VI. CONCLUSION

This paper introduces a new high step-up interleaved DC-DC converter that utilizes coupled inductor technology. It combines the converter's working principle, steady-state analysis, and experimental results to highlight its characteristics and advantages. The first advantage is the high voltage gain achieved through the series connection of capacitors and secondary windings of coupled inductors. Secondly, there is a common ground between the input and output voltages, thus reducing the risk of leakage current and greatly simplifying the control system. Thirdly, the clamping circuit absorbs the leakage voltage spikes, resulting in relatively low voltage stresses on switches and diodes. It is experimentally proved to have high conversion efficiency, effectiveness and stability under different system frequency conditions. Based on the above characteristics, the proposed converter is valuable to be used on renewable energy generation systems.

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AUTHORS' CONTRIBUTIONS

Yin Chen: conceptualization, methodology, data curation, software, original draft preparation. Haibin Li: reviewing, and editing. Tao Jin: conceptualization, methodology, data curation, reviewing, and editing. All authors read and approved the final manuscript.

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AVAILABILITY OF DATA AND MATERIALS

Not applicable.

DECLARATIONS

Competing interests:The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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