Tri-state Modulation with Operating Losses Minimization for a Soft-switching Bidirectional DC-DC Converter

Jiaqi Yu, Yong Li, *Senior Member*, *IEEE*, Jianghu Wan, Feng Zhou, Mingmin Zhang, and Lihua Cao

***Abstract*—This paper introduces a tri-state modulation technique for a soft-switching bidirectional DC-DC converter (BDC). This method maintains the soft-switching condition and introduces a freewheeling interval that reduces the rise and fall times of the inductor current, effectively suppressing inductor current ripples. Additionally, the tri-state modulation provides an extra degree of freedom, enabling optimization for reduced operating losses. The paper details the operation principles of tri-state modulation in both buck and boost modes and discusses optimization strategies for minimizing losses. An experimental setup is developed to validate the tri-state modulation approach, where switching waveforms and efficiency are measured. The experimental results confirm that the proposed method achieves soft-switching conditions, suppresses inductor current ripples, and provides higher efficiency compared to conventional hard-switching BDC and typical soft-switching BDC.**

***Index Terms*—Bidirectional DC-DC converter, soft-switching, inductor current ripples, tri-state control, efficiency improvement.**

NOMENCLATURE

BDC	bidirectional DC-DC converter
ZVS	zero-voltage-switching
ZCS	zero-current-switching
DCM	discontinuous conduction mode

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I. INTRODUCTION

Bidirectional DC-DC converter (BDCs), capable of delivering energy in both directions, are widely utilized as interface circuits in various applications, such as photovoltaic systems [1], [2], uninterrupted power supplies [3], [4], and electric vehicles [5], [6]. BDC can be derived from a unidirectional DC-DC converter by replacing the diode with a synchronous rectification switch. However, this modification introduces significant switching and reverse recovery losses [7]. Furthermore, distributed loss analysis of conventional BDCs indicates that core losses constitute the largest portion of total losses under light load conditions [8], [9]. Therefore, reducing core losses is essential to enhance efficiency.

To mitigate switching losses and reverse recovery losses, several soft-switching strategies have been proposed, which can be broadly categorized into three types: BDCs without auxiliary circuits, BDCs with passive auxiliary circuits, and BDCs with active auxiliary circuits. BDCs without auxiliary circuits utilize a triangular current mode or quasi-square wave operation to achieve zero-voltage-switching (ZVS) for switches without adding extra components [10], [11]. However, these operational modes result in significant inductor current ripples, necessitating a larger capacitor to maintain low output voltage ripple, leading to increased core losses. While variable frequency control techniques have been implemented in [12] to reduce the ripples under light load conditions, they also introduce additional control complexity. Moreover, as the load increases, the switching frequency must decrease to ensure adequate energy transmission, which exacerbates core losses and degrades output voltage quality. To address these limitations, BDCs with passive auxiliary circuits but without switches have been introduced.

In [13], two pairs of small auxiliary inductors and capacitors are introduced to achieve ZVS for all transistors. The use of current circulation through these auxiliary components helps minimize inductor current

ripples. However, the effectiveness of the soft-switching range in BDCs with passive auxiliary circuits is highly dependent on the converter's operating duty cycle and load conditions, making them effective only within a specific load range [14], [15]. Conversely, BDCs with active auxiliary circuits use active control switches to achieve ZVS for all switches. For example, in [16], a BDC with an active auxiliary circuit employing a leakage inductor as the auxiliary inductor is proposed. This design provides the benefits of soft-switching and a reduced number of magnetic cores. Unfortunately, in certain topologies, the turns ratios are fixed, limiting the range of soft-switching operation. Moreover, since inductor current ripples are not mitigated, the converter continues to suffer from significant core losses. In [17], a fully switched BDC with an auxiliary resonant circuit, consisting of a resonant element and a single auxiliary switch, is presented. This resonant circuit enables soft-switching for all switches. However, operating in resonance leads to high reactive currents, which cause additional losses. In [18]–[20], a typical soft-switching BDC is proposed, offering several advantages: 1) soft-switching is achieved for all auxiliary switches; 2) the voltage stress on auxiliary switches is lower than in previous BDC designs; and 3) no additional voltage or current stress is placed on the main switches. However, this approach is also limited by the absence of strategies to suppress inductor current ripples and reduce core losses.

Several studies have explored methods to enhance efficiency by suppressing inductor current ripples [21]–[24]. In [21], a tri-state boost converter is proposed to eliminate the right-half-plane zero in the converter's small-signal control-to-output transfer function, thereby expanding bandwidth and reducing inductor current ripples through tri-state control. In [22], current ripple reduction is achieved under light load conditions using a dual-pole switching method without the need for increased inductance. A soft-switching tri-state boost converter is introduced in [23], where comparative results indicate that its performance surpasses that of both the soft-switching boost converter and the tri-state boost converter. In [24], an interleaved tri-state boost converter is proposed to further suppress inductor current ripples and enhance dynamic response. The key advantage of BDCs with tri-state modulation lies in their ability to reduce inductor current ripples while achieving a faster dynamic response. However, these converters also experience relatively higher reverse recovery and hard-switching losses compared to those in [18].

Therefore, this paper introduces a tri-state modulation for a typical soft-switching BDC aimed at suppressing inductor current ripples while maintaining the soft-switching condition. By incorporating a free-wheeling interval within the tri-state modulation, this approach effectively suppresses inductor current ripples and minimizes losses across various output power conditions. The main contributions of this paper are as follows:

1) A tri-state modulation method is proposed to reduce the ripple current flowing in the main inductor.

2) A comprehensive analysis of power loss is conducted to develop a detailed loss model.

3) The loss model is executed, and a corresponding figure is generated to determine the optimal duty cycle for the auxiliary switch, thereby maximizing efficiency.

The structure of this paper is as follows. Section II details the operating principles of the BDC with tri-state modulation. Section III discusses design considerations and strategies for minimizing losses. Section IV presents the experimental results, and conclusions are given in Section V.

II. Operation Principles with Tri-State Modulation

The configuration of the typical soft-switching BDC is depicted in Fig. 1. This circuit comprises a conventional hard-switching BDC integrated with a simple auxiliary circuit. The conventional hard-switching BDC features two switches (S_1 and S_2) and a main inductor L, while the auxiliary circuit includes a pair of auxiliary switches (S_{a1} and S_{a2}) and a small auxiliary inductor L_r. Depending on the direction of power flow, this soft-switching BDC can operate in either buck or boost mode. In Fig. 1, the positive current flow direction is shown for the buck mode. Conversely, in boost mode, the positive current flow direction is opposite to that of buck mode.

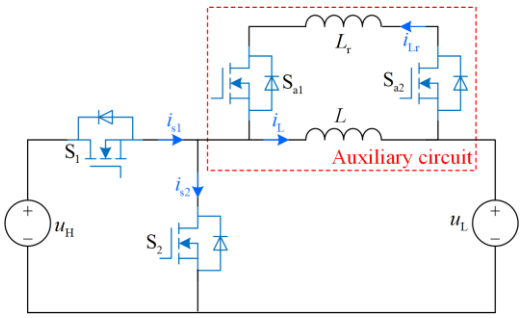


Fig. 1. Configuration of the typical soft-switching BDC.

In buck mode, the BDC operates in three distinct modes: 1) main inductor charging mode, where switch S_1 is on and S_2 is off, causing the current in the main inductor i_L to increase due to the positive voltage $(u_H - u_L)$; 2) main inductor discharging mode, in which S_1 is off and S_2 is on, leading to a decrease in inductor current i_L due to the applied negative voltage $-u_L$; 3) free-wheeling mode, where both S_1 and S_2 are off, and the auxiliary switches S_{a1} and S_{a2} are on. In this

mode, the inductor current freewheels through the auxiliary circuit, and the current is assumed to be constant. This freewheeling interval introduces an additional operational state for the BDC, which narrows the rise and fall times of the inductor current and helps reduce inductor current ripples. In boost mode, the BDC operates similarly, with the state of S_1 and S_2 reversed.

A. Operation Principle with Tri-state Modulation in Buck Mode

In buck mode, a BDC with tri-state modulation operates through six distinct intervals during each switching period. The conduction circuit in buck mode is illustrated in Fig. 2, and the corresponding key theoretical waveforms are depicted in Fig. 3(a).

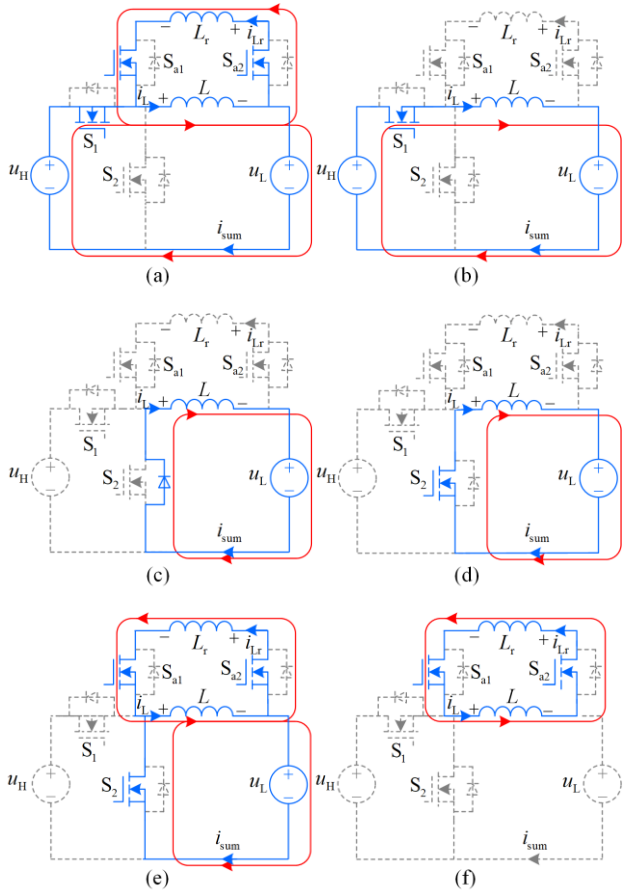


Fig. 2. Conduction circuit for all intervals in the buck mode. (a) Interval 1. (b) Interval 2. (c) Interval 3. (d) Interval 4. (e) Interval 5. (f) Interval 6.

The auxiliary switches S_{a1} and S_{a2} have the same on-off action and drive signals. Before the initial interval, only the auxiliary circuit is active: both S_1 and S_2 are off, while S_{a1} and S_{a2} are on. In this state, the currents in both the main inductor and the auxiliary inductor are equal and circulate through the auxiliary circuit. The subsequent intervals are characterized by various combinations of switch states, which are detailed in the conduction circuits provided.

Interval 1: [$t_0 - t_1$, Fig. 2(a)]: At time t_0, the main switch S_1 is turned on, causing the current in the main inductor i_L to begin increasing due to the positive voltage $(u_H - u_L)$. Concurrently, the current in the auxiliary inductor i_{Lr} decreases as a result of the negative voltage $(u_L - u_H)$. The inductor currents during this interval can be expressed as follows:

$$i_L(t) = i_L(t_0) + (u_H - u_L)(t - t_0)/L \quad (1)$$

$$i_{Lr}(t) = i_{Lr}(t_0) + (u_L - u_H)(t - t_0)/L \quad (2)$$

During this stage, S_1 experiences only capacitive turn-on losses, and the turn-on voltage across S_1 is $u_H - u_L$.

Interval 2: [$t_1 - t_2$, Fig. 2(b)]: At time t_1, the current i_{Lr} in the auxiliary inductor decays to zero. To avoid reversal of the auxiliary current, the auxiliary switches S_{a1} and S_{a2} are turned off, rendering the auxiliary circuit inactive. As a result, the system behaves similarly to a conventional buck circuit: with the main switch S_1 still on, the current i_L in the main inductor continues to increase, maintaining the same slope as in the previous interval.

$$i_L(t) = i_L(t_1) + (u_H - u_L)(t - t_1)/L, i_{Lr}(t) = 0 \quad (3)$$

Interval 3: [$t_2 - t_3$, Fig. 2(c)]: This stage introduces a dead time to prevent short-circuiting of the input voltage source. At time t_2, the main switch S_1 is turned off, causing the body diode of S_2 to become forward-biased and begin conducting. As a result, the terminal voltage of S_2 drops to zero, and the current i_L in the main inductor reaches its maximum value I_P. Subsequently, i_L begins to decrease due to the application of the negative voltage $-u_L$.

$$i_L(t) = i_L(t_2) - u_L(t - t_2)/L, i_{Lr}(t) = 0 \quad (4)$$

Interval 4: [$t_3 - t_4$, Fig. 2(d)]: At time t_3, switch S_2 is turned on. During this interval, S_2 operates in its Ohmic region, and the current i_L in the main inductor gradually decreases with the same slope as in the previous intervals.

$$i_L(t) = i_L(t_3) - u_L(t - t_3)/L, i_{Lr}(t) = 0 \quad (5)$$

Interval 5: [$t_4 - t_5$, Fig. 2(e)]: At time t_4, switches S_{a1} and S_{a2} are turned on, activating the auxiliary circuit. The current i_L in the main inductor continues to decrease with a slope of $-u_L/L$. Due to the positive voltage u_L, the current i_{Lr} in the auxiliary inductor begins to increase. During the turn-on transient of S_{a1} and S_{a2}, S_{a1} incurs capacitive turn-on losses, whereas S_{a2} experiences ZVS during its turn-on.

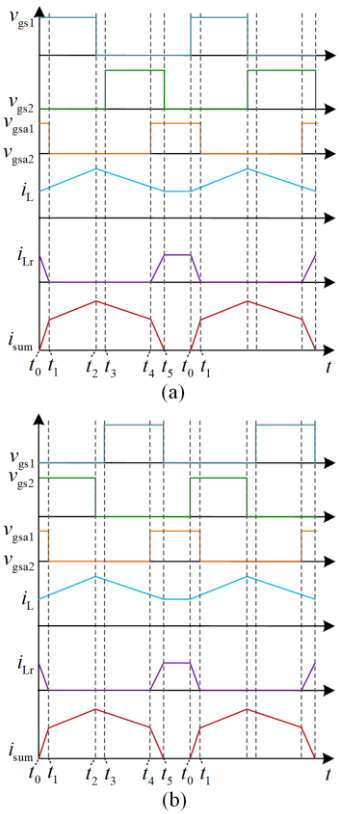


Fig. 3. The key theoretical waveforms in buck and boost modes. (a) Buck mode. (b) Boost mode.

$$i_L(t) = i_L(t_4) - u_L(t - t_4)/L \tag{6}$$

$$i_{Lr}(t) = u_L(t - t_4)/L_r \tag{7}$$

Interval 6: [$t_5 - t_6$, Fig. 2(f)]: At time t_5, the current i_{Lr} in the auxiliary inductor reaches its maximum value and equals i_L. Simultaneously, S_2 is turned off to prevent the output current from flowing back into the input side. S_2 achieves zero-current-switching (ZCS) during this turn-off, resulting in no reverse recovery losses since all current is circulating within the auxiliary circuit. Additionally, due to the extremely low channel resistance of S_{a1} and S_{a2}, the voltages across both the main inductor and auxiliary inductor are nearly zero, causing i_L and i_{Lr} to remain approximately constant.

$$i_L(t) = i_{Lr}(t) = I_r \tag{8}$$

To visually illustrate the reduction in inductor current ripples, Fig. 4 compares the inductor current waveforms of a BDC with tri-state modulation and a conventional hard-switching BDC in buck mode. The figure shows that the introduction of the free-wheeling mode (d_fT) compresses the inductor's charging and discharging times. Consequently, the average inductor current in the BDC with tri-state modulation is higher than that in the conventional hard-switching BDC. Additionally, the inductor current ripples are significantly smaller in the BDC with tri-state modulation compared to the hard-switching BDC.

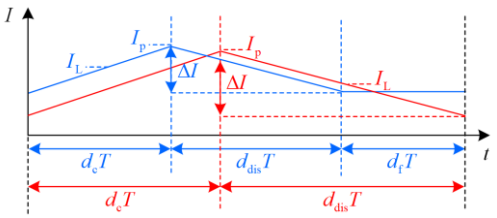


Fig. 4. The principle of inductor current ripples suppression.

B. Operation Principle with Tri-state Modulation in Boost Mode

When the BDC operates in boost mode, energy is transferred from the low-voltage side to the high-voltage side. Similar to buck mode, boost mode involves six operating intervals per switching period, with the key theoretical waveforms depicted in Fig. 3(b). The corresponding conduction circuits for all intervals are illustrated in Fig. 5. For simplicity, the reference current direction in boost mode is opposite to that in buck mode. Since boost mode is essentially the reverse process of buck mode, its operational principles mirror those of buck mode. Consequently, the description of boost mode operation is presented here in a brief overview.

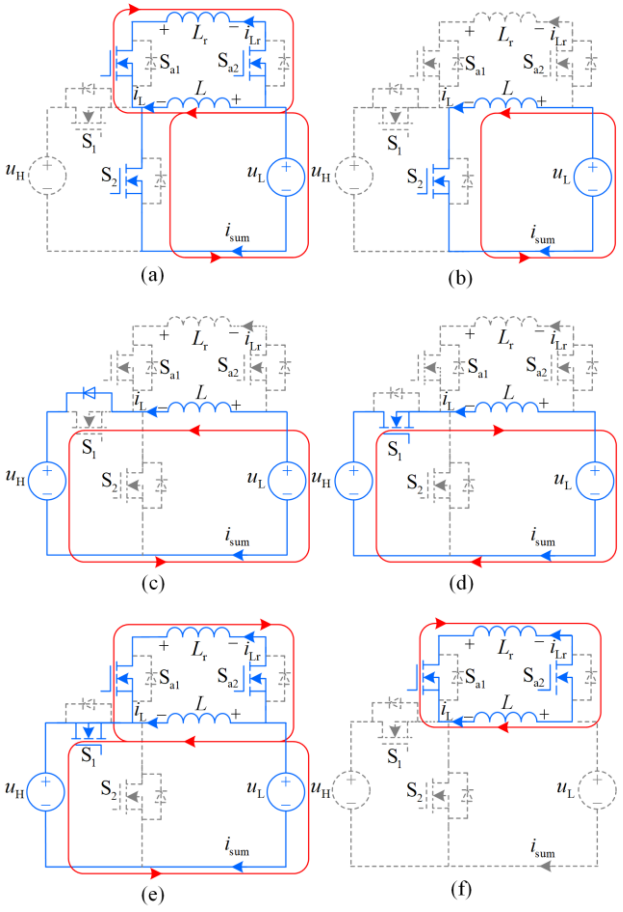


Fig. 5. Conduction circuit for all intervals in the boost mode. (a) Interval 1. (b) Interval 2. (c) Interval 3. (d) Interval 4. (e) Interval 5. (f) Interval 6.

Interval 1: [$t_0 - t_1$, Fig. 5(a)]: At time t_0, switch S_2 is activated, applying voltage u_L across the main inductor L and $-u_L$ across the auxiliary inductor L_r. As a result, the current through the main inductor i_L begins to increase with a slope of u_L/L, while the current through the auxiliary inductor i_{Lr} decreases with a slope of $-u_L / L_r$. The equations governing i_L and i_{Lr} during this interval are given by:

$$i_L(t) = i_L(t_0) + u_L(t - t_0) / L \tag{9}$$

$$i_{Lr}(t) = i_{Lr}(t_0) - u_L(t - t_0) / L_r \tag{10}$$

This interval concludes when i_{Lr} decays to zero. Throughout this period, switch S_2 incurs only capacitive turn-on losses, with the turn-on voltage being u_L.

Interval 2: [$t_1 - t_2$, Fig. 5(b)]: At t_1, switches S_{a1} and S_{a2} are turned off under ZCS conditions, rendering the auxiliary circuit inactive. The inductor current i_L continues to increase due to the positive voltage u_L. The equations governing the inductor current during this interval are:

$$i_L(t) = i_L(t_1) + u_L(t - t_1) / L, i_{Lr}(t) = 0 \tag{11}$$

Interval 3: [$t_2 - t_3$, Fig. 5(c)]: At t_2, switch S_2 is turned off, causing the body diode of S_1 to become forward biased and start conducting. As a result, $(u_L - u_H)$ is applied across the inductor L. The inductor current i_L reaches its maximum and then begins to decrease. The equations describing the inductor behavior during this interval are:

$$i_L(t) = i_L(t_2) + (u_L - u_H)(t - t_2) / L, i_{Lr}(t) = 0 \tag{12}$$

Interval 4: [$t_3 - t_4$, Fig. 5(d)]: At t_3, switch S_1 is turned on under ZVS conditions. The voltage across the main inductor L remains at $(u_L - u_H)$, so the inductor current i_L continues to decrease with the same slope in the previous interval. The equation for this interval is given by:

$$i_L(t) = i_L(t_3) + (u_L - u_H)(t - t_3) / L, i_{Lr}(t) = 0 \tag{13}$$

Interval 5: [$t_4 - t_5$, Fig. 5(e)]: At t_4, switches S_{a1} and S_{a2} are turned on, activating the auxiliary circuit. Consequently, due to the positive voltage $(u_H - u_L)$ across the auxiliary inductor, the auxiliary inductor current i_{Lr} begins to increase from zero, while i_L continues to decrease. The equations governing the current in the inductor are given as:

$$i_L(t) = i_L(t_4) + (u_L - u_H)(t - t_4) / L \tag{14}$$

$$i_{Lr}(t) = (u_H - u_L)(t - t_4) / L_r \tag{15}$$

During the turn-on phase of S_{a1} and S_{a2}, switch S_{a2} only experiences only capacitive turn-on losses, where the turn-on voltage is $u_H - u_L$, while S_{a1} is turned on under ZVS conditions.

Interval 6: [$t_5 - t_6$, Fig. 5(f)]: At t_5, i_L and i_{Lr} are equal. Simultaneously, switch S_1 is turned off under ZCS conditions, resulting in current circulation only within the auxiliary circuit. Due to the small channel resistance of S_{a1} and S_{a2}, the voltage across inductors L and L_r are nearly zero, causing the currents i_L and i_{Lr} to remain approximately constant.

$$i_L(t) = i_{Lr}(t) \tag{16}$$

III. Design Considerations and Losses Minimization

This section outlines the design process for the key components, including the main inductor L and auxiliary inductor L_r, as well as the critical factor d_f for minimizing losses. The BDC with tri-state modulation is designed under the following conditions: high-side voltage u_H of 45 V, low-side voltage u_L of 30 V, switching frequency f_s of 100 kHz, and output power P_o of 200 W. The design methods for both buck and boost modes are analogous; hence, only the design methodology for buck mode is detailed here.

A. Design of L and L_r

To ensure continuous inductor current across a broad load range, the minimum value of the main inductor L should be determined under conditions where inductor current ripple is at its maximum. Therefore, the minimum value of L is initially designed in a manner similar to a conventional PWM buck converter, which can be calculated using:

$$L \geqslant u_H^2 d_c^2 (1 - d_c) / (2 P_o f_s) \tag{17}$$

Choosing an appropriate L_r is crucial as it influences the inverse transmission energy, the rise and fall times of i_{Lr}, and the reverse recovery losses of the parasitic anti-parallel diode in the synchronous rectification switch. In steady state, the switching period T can be divided into three parts based on the operating modes: $d_c T$ for main inductor charging mode (intervals 1 and 2), $d_{dis} T$ for main inductor discharging mode, and $d_f T$ for free-wheeling mode. Ignoring the dead time and switching transient effects, the duty ratios for the buck operation, d_c, d_{dis}, and d_f satisfy the following equation:

$$\begin{cases} t_2 - t_0 = d_c T,\ t_5 - t_2 = d_{dis} T \\ t_0 - t_5 = d_f T,\ d_c + d_{dis} + d_f = 1 \end{cases} \tag{18}$$

Using the principles of inductor volt-second balance, the voltage transfer ratio k can be derived as follows:

$$k = u_L / u_H = d_c / (d_c + d_{dis}) \tag{19}$$

During the circulation, the current i_{Lr} flows in the opposite direction of i_L, resulting in energy being transferred back to the input side. According to the

principle of energy conservation over one switching period, the total energy transferred by the main inductor, along with the reverse energy transferred by the auxiliary inductor, must equal the output energy. This relationship can be expressed as:

$$I_{\mathrm{L}}u_{\mathrm{L}}(1-d_{\mathrm{f}})T - I_{\mathrm{r}}u_{\mathrm{L}}d_{\mathrm{r}}T/2 = P_{\mathrm{o}}T \tag{20}$$

where I_{L} represents the average current of the main inductor during the charging and discharging phases; I_{r} denotes the peak current of the auxiliary inductor; and $d_{\mathrm{r}}T$ indicates the charging time of the auxiliary inductor, which is equal to its discharging time. Additionally, based on the current waveforms of i_{L} and i_{Lr}, the estimates for I_{L} and I_{r} can be calculated as follows:

$$\begin{cases} I_{\mathrm{L}} = I_{\mathrm{r}} + u_{\mathrm{L}}d_{\mathrm{dis}}T/(2L) \\ I_{\mathrm{r}} = u_{\mathrm{L}}d_{\mathrm{r}}T/L_{\mathrm{r}} \end{cases} \tag{21}$$

By substituting (18), (19), and (21) into (20), a quadratic equation in terms of d_{r} can be obtained. This quadratic equation is expressed as follows:

$$\frac{u_{\mathrm{L}}^2T}{2L_{\mathrm{r}}}d_{\mathrm{r}}^2 - \frac{u_{\mathrm{L}}^2T(1-d_{\mathrm{f}})}{L_{\mathrm{r}}} + P_{\mathrm{o}} - \frac{u_{\mathrm{L}}^2d_{\mathrm{dis}}T(1-d_{\mathrm{f}})}{2L} = 0 \tag{22}$$

Given that $\Delta > 0$ and $0 < d_{\mathrm{r}} < d_{\mathrm{dis}}$, the following conditions must be satisfied for the quadratic equation:

$$\begin{cases} L \succ (1-k)(1-d_{\mathrm{f}})^2u_{\mathrm{L}}^2T/(2P_{\mathrm{o}}) \\ ((1-k^2)L + (1-k)L_{\mathrm{r}})/LL_{\mathrm{r}} \succ 2P_{\mathrm{o}}/(u_{\mathrm{L}}^2T(1-d_{\mathrm{f}})^2) \end{cases} \tag{23}$$

Given the range $0 < d_{\mathrm{f}} < 1$, the maximum value of the main inductor in (23) will be larger than that in (17). Therefore, the inductance values for both the main inductor and the auxiliary inductor can be determined based on (23). For this paper, the inductance values are chosen as $L = 33\ \mu\mathrm{H}$ and $L_{\mathrm{r}} = 2\ \mu\mathrm{H}$.

By solving (22), the parameters d_{r}, I_{L}, and I_{r} are calculated as follows:

$$d_{\mathrm{r}} = (1-d_{\mathrm{f}}) - \sqrt{(1-d_{\mathrm{f}})^2 + \frac{L_{\mathrm{r}}}{L}d_{\mathrm{dis}}(1-d_{\mathrm{f}}) - \frac{2P_{\mathrm{o}}L_{\mathrm{r}}}{u_{\mathrm{L}}^2T}} \tag{24}$$

$$I_{\mathrm{r}} = \frac{u_{\mathrm{L}}T}{L_{\mathrm{r}}}\left(1-d_{\mathrm{f}} - \sqrt{(1-d_{\mathrm{f}})^2 + \frac{L_{\mathrm{r}}}{L}d_{\mathrm{dis}}(1-d_{\mathrm{f}}) - \frac{2P_{\mathrm{o}}L_{\mathrm{r}}}{u_{\mathrm{L}}^2T}}\right) \tag{25}$$

$$I_{\mathrm{L}} = \frac{u_{\mathrm{L}}T}{L_{\mathrm{r}}}\left(1-d_{\mathrm{f}} - \sqrt{(1-d_{\mathrm{f}})^2 + \frac{L_{\mathrm{r}}}{L}d_{\mathrm{dis}}(1-d_{\mathrm{f}}) - \frac{2P_{\mathrm{o}}L_{\mathrm{r}}}{u_{\mathrm{L}}^2T}}\right) + \frac{u_{\mathrm{L}}d_{\mathrm{dis}}T}{2L} \tag{26}$$

B. Design of d_{f} Consideration for Losses Minimization

To achieve optimal performance with minimized losses, it is crucial to accurately calculate the total losses. The total losses in the BDC can be categorized into two primary types: losses associated with switches and losses associated with inductors. Losses of switches include conduction, turn-on, and turn-off losses.

1) Conduction Losses

With a driving voltage of 12 V, the on-resistance R_{ds} of MOSFETs is approximately 70 mΩ. During the interval $[0, d_{\mathrm{c}}T]$, the slope of the inductor current i_{L} is given by $(u_{\mathrm{H}} - u_{\mathrm{L}})/L$, and it goes through the point $(d_{\mathrm{c}}T/2, I_{\mathrm{L}})$. Consequently, the RMS value of the inductor current I_{Ls1} is calculated as:

$$I_{\mathrm{Ls1}} = \sqrt{d_{\mathrm{c}}I_{\mathrm{L}}^2 + (u_{\mathrm{H}} - u_{\mathrm{L}})^2d_{\mathrm{c}}^3T^2/(12L^2)} \tag{27}$$

Accordingly, the conduction losses for switch $\mathrm{S_l}$ are given by:

$$P_{\mathrm{cs1}} = d_{\mathrm{c}}I_{\mathrm{L}}^2R_{\mathrm{ds}} + (u_{\mathrm{H}} - u_{\mathrm{L}})^2d_{\mathrm{c}}^3T^2R_{\mathrm{ds}}/(12L^2) \tag{28}$$

Similarly, the conduction losses for switch $\mathrm{S_2}$ are:

$$P_{\mathrm{cs2}} = d_{\mathrm{dis}}I_{\mathrm{L}}^2R_{\mathrm{ds}} + u_{\mathrm{L}}^2d_{\mathrm{dis}}^3T^2R_{\mathrm{ds}}/(12L^2) \tag{29}$$

Similarly, the conduction losses for both $\mathrm{S_{a1}}$ and $\mathrm{S_{a2}}$ are identical, resulting in the total conduction losses being:

$$P_{\mathrm{csa12}} = 2(d_{\mathrm{f}}I_{\mathrm{r}}^2 + I_{\mathrm{r}}^3L_{\mathrm{r}}u_{\mathrm{H}}/(3u_{\mathrm{L}}(u_{\mathrm{H}} - u_{\mathrm{L}})T))R_{\mathrm{ds}} \tag{30}$$

2) Turn-on Losses

The turn-on losses encompass the capacitive losses associated with $\mathrm{S_l}$ and $\mathrm{S_{a1}}$. Assuming each switch has an identical capacitance of $C_{\mathrm{s}} = 1\ \mathrm{nF}$, the capacitive turn-on losses for $\mathrm{S_l}$ and $\mathrm{S_{a1}}$ are calculated as follows:

$$P_{\mathrm{tns1}} = C_{\mathrm{s}}(u_{\mathrm{H}} - u_{\mathrm{L}})^2f_{\mathrm{s}}/2 \tag{31}$$

$$P_{\mathrm{tnsa1}} = C_{\mathrm{s}}u_{\mathrm{L}}^2f_{\mathrm{s}}/2 \tag{32}$$

3) Turn-off Losses

All switches, except $\mathrm{S_l}$, are turned off under ZCS conditions. Based on literature [23], the turn-off losses of $\mathrm{S_l}$ are influenced by the drain-source voltage u_{ds}, the fall time t_{f}, and the maximum inductor current i_{Lmax} during the turn-off process. These losses can be expressed as follows:

$$P_{\mathrm{tfs1}} = \frac{1}{2}u_{\mathrm{ds}}i_{\mathrm{Lmax}}t_{\mathrm{f}}f_{\mathrm{s}} = \frac{1}{2}u_{\mathrm{H}}\left(I_{\mathrm{L}} + \frac{u_{\mathrm{L}}T}{6L}(1-d_{\mathrm{f}})\right)t_{\mathrm{f}}f_{\mathrm{s}} \tag{33}$$

where t_{f} represents 20 ns, as specified in the switch's datasheet.

4) Core Losses

The current ripples induce losses in the inductor core. For a core material chosen as Kool Mμ-77350A7, the core losses per unit volume can be described by the following equation:

$$P_{\mathrm{fe}} = 91.58\mathrm{e}^{-6}B^{2.2}f_{\mathrm{s}}^{1.63} \tag{34}$$

where B denotes flux density. Based on the expression of B and the empirical formula for L, the flux density B can be derived as follows:

$$B = \sqrt{\mu L/V_{\mathrm{e}}}\Delta I \tag{35}$$

where μ represents the magnetic permeability; L is the inductance value; V_e is the core volume; and ΔI denotes the current ripple. In buck mode, the current ripple of the main inductor is given by:

$$\Delta I = u_L(u_H - u_L)(1-d_f)T/(Lu_H) \tag{36}$$

Accordingly, the core losses in the main inductor are expressed as follows [25]:

$$P_{feL} = 91.58e^{-6}\left(\sqrt{\frac{\mu L}{V_e}}\left(\frac{u_L(u_H-u_L)(1-d_f)T}{Lu_H}\right)\right)^{2.2} f_s^{1.63}V_e \tag{37}$$

In contrast, the SER2012 high-current shielded power inductor is chosen for the auxiliary inductor. According to its datasheet, the losses for the auxiliary inductor are 189 MW at $L_r = 2\ \mu H$ and $I_r = 12\ A$.

The conduction, turn-on, and turn-off losses for the four switches, along with the core losses of the main and auxiliary inductors, are summarized in Table I. As a result, the total losses in buck mode are given by:

$$P_{total} = P_{cs1} + P_{cs2} + P_{csa12} + P_{tns1} + P_{tnsa2} + P_{tfs1} + P_{feL} + P_{feLr} \tag{38}$$

TABLE I
LOSSES OF THE BDC WITH TRI-STATE MODULATION IN BUCK MODE

		Conduction losses	Turn-on loss	Turn-off losses
Losses of switches	S_1	Eq. (28)	Eq. (31)	Eq. (33)
	S_2	Eq. (29)		
	S_{a1}	Eq. (30)	Eq. (32)	
	S_{a2}	Eq. (30)		
Losses of inductors		Eq. (37)		

Given the circuit parameters of the BDC, such as L = 33 μH, $L_r = 2\ \mu H$, $\mu = 60$, and $V_e = 2280\ mm^3$, the total losses are a function of d_f and P_o. Therefore, by adjusting the duty ratio d_f, the total losses P_{total} can be optimized, allowing for the minimization of losses across various load conditions.

Figure 6 illustrates P_{total} as a function of d_f and P_o. It is evident that P_o increases, and the range of d_f decreases. This can be explained by energy transmission dynamics: as P_o rises, d_c must also increase, leading to a reduction in the range of d_f. Furthermore, total losses increase with P_o, reaching their peak when $P_o = 200$ and $d_f = 0.7$. To minimize losses, a large d_f is beneficial at lower output power, while a smaller d_f is preferable at higher output power.

Under these conditions, the minimum losses are represented by the red area in Fig. 6, indicating that the approximate optimal range for d_f is between 0.3 and 0.8. At a specific output power P_o, total losses initially decrease with increasing d_f but eventually rise as d_f continues to increase. This behavior is further clarified in Fig. 7, which illustrates the relationship between P_{total} and d_f at various P_o levels. The figure shows that an optimal d_f exists for minimizing losses. In practice, this optimal d_f is determined by solving for the minimum value of (38).

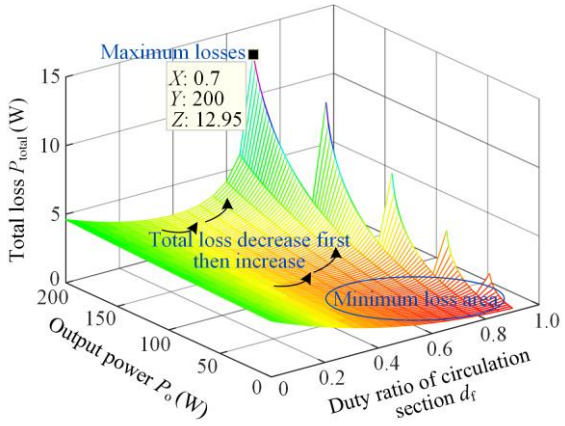


Fig. 6. Total losses P_{total} as a function of the d_f and P_o.

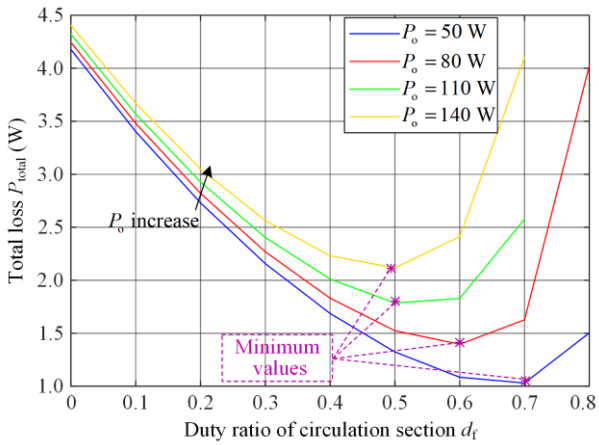


Fig. 7. Relationship of P_{total} and d_f at different P_o.

Additionally, the value of d_f impacts the maximum inductor current, which in turn influences the saturation current and the volume of the inductor. Consequently, d_f must be constrained by the maximum allowable inductor current. The maximum inductor current I_{Lmax} is given by the following equation:

$$I_{Lmax} = \frac{u_L T}{L_r}\left(1-d_f-\sqrt{(1-d_f)^2+\frac{L_r}{3L}(1-d_f)^2-\frac{2P_oL_r}{u_L^2T}}\right)+\frac{u_L T}{3L}(1-d_f) \tag{39}$$

Figure 8 illustrates the relationship between I_{Lmax} and d_f across different output power levels P_o. As d_f increases, I_{Lmax} also rises. Beyond $d_f = 0.6$ and $d_f = 0.7$, the increase in I_{Lmax} becomes more pronounced, leading to a larger inductor volume. To balance performance and cost, the maximum d_f is selected

as 0.6. Consequently, for the given circuit parameters, d_f ranges from 0.3 to 0.6. This loss analysis is applicable to boost mode as well, though it is not detailed in this paper to avoid redundancy.

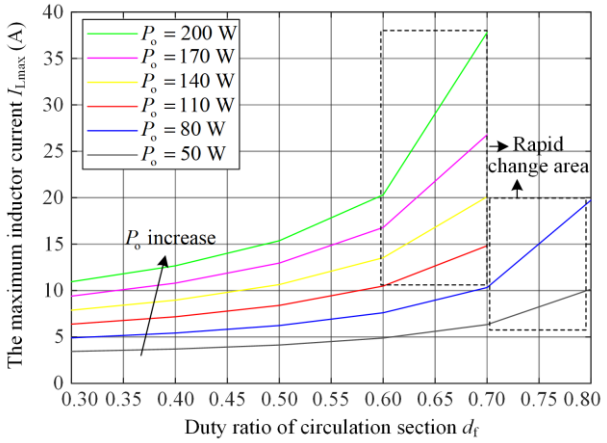


Fig. 8. Relationship of I_{Lmax} and d_f at different P_o.

To further demonstrate the advantages of this method, Table II presents a comparison between the proposed and other converters. Compared to the design in [23], the proposed approach reduces the number of components and lowers the voltage stress on the main switch obtained in the BDC with proposed tri-state modulation. In comparison with the design in reference [26], it achieves reductions in inductor current ripples, current stress on the main switch, and voltage stress on the auxiliary switch.

TABLE II
COMPARISON RESULTS BETWEEN THE PROPOSED AND OTHER TRI-STATE CONVERTERS

	Features	Ref[23]	Ref[26]	Proposed
Number of devices	Circuit type	Boost	Buck	Bidirection
	Switches	2	4	4
	Auxiliary inductor	1		1
	Auxiliary capacitor	C_a		
	Auxiliary diode	4		
	Inductor current ripples ($\Delta I/2$)		$\frac{(u_H-u_L)}{2L_f}d_c$	
Voltage stress in buck mode	Main switch		u_H	u_H
	Auxiliary switch		$\mathrm{Max}\{u_H-u_L,u_L\}$	u_L
Current stress in buck mode	Main switch		δ	δ
	Auxiliary switch		I_r	I_r
Voltage stress in boost mode	Main switch	u_H+u_{ca}		u_H
	Auxiliary switch	u_H-u_L		$\mathrm{Max}\{u_H-u_L,u_L\}$
Current stress in boost mode	Main switch	δ		δ
	Auxiliary switch	I_r		I_r

Note: $\delta=\frac{P}{u_L(1-d_f)}+\frac{\Delta I}{2}$.

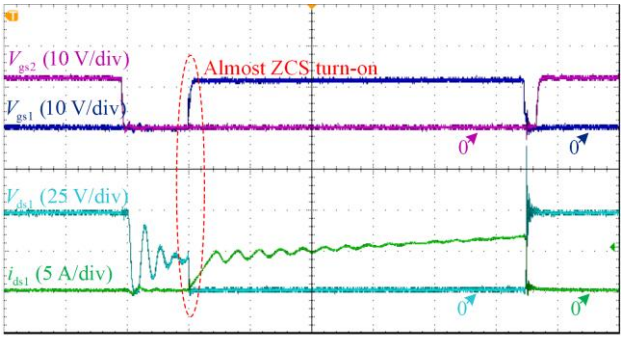
IV. EXPERIMENT VERIFICATION

This paper primarily focuses on reducing inductor current ripples and minimizing losses for a soft-switching BDC under varying output power conditions. To validate these functions, an experimental setup was created using a prototype circuit, resistor load, DC power supply, oscilloscope, power analyzer, and current probe. The prototype circuit is constructed based on the parameters outlined in Section III. The MOSFET IRFP250M is used for all switches, selected based on permissible voltage and current stresses. The control unit is the STM32F405RGT6 microprocessor with on Cortex-M4 core from STMicroelectronics. The detailed hardware parameters are as follows: high-side voltage u_H is 45 V, low-side voltage u_L is 30 V, switching frequency f_s is 100 kHz, output power P_o is 200 W, main inductance $L = 33$ μH, auxiliary inductance $L_r = 2$ μH, magnetoconductivity $\mu = 60$, and the core material is Mu-77350A7. The experimental setup and circuit design are illustrated in Fig. 9.

Fig. 9. Experimental platform and the implemented prototype circuit.

A. Switching Losses Elimination

The measured waveforms, including driver signals V_{gsn}, drain-to-source voltage V_{dsn}, and drain-to-source i_{dsn} (n = 1, 2, a1, a2) of the implemented BDC in both buck and boost modes are depicted in Fig. 10 and 11, respectively.



(a)

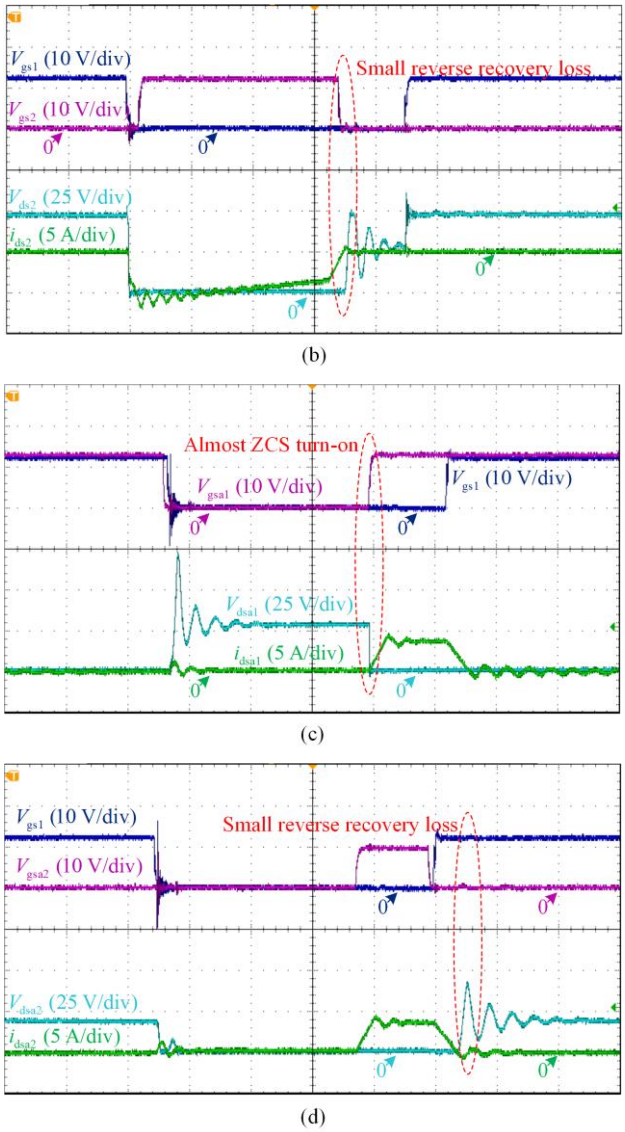


Fig. 10. Switching waveforms in buck mode. (a) Almost ZCS of S_1. (b) Small reverse recovery losses during S_2 turn-off process. (c) Almost ZCS of S_{a1}. (d) Small reverse recovery losses during S_{a2} turn-off process.

In Fig. 10(a), nearly ZCS is achieved for switch S_1 during turn-on, as the drain-to-source current i_{ds1} remains zero before the gate signal V_{gs1} is applied and only starts to increase after V_{ds1} drops to zero. Figure 10(b) illustrates the turn-off process of switch S_2, where the reverse recovery losses of the body diode are significantly reduced due to the minimal reverse recovery current.

Similarly, Fig.10(c) shows that almost ZCS is achieved for switch S_{a1} at turn-on since i_{dsa1} is zero before the trigger signal starts, ensuring no overlap between current and voltage. Figure 10(d) presents the turn-off process of switch S_{a2}, where the body diode reverse recovery losses are also significantly minimized due to the small i_{dsa2} during the reverse recovery process. In boost mode, both S_2 and S_{a2} similarly achieve almost ZCS turn-on conditions, and the reverse recovery losses of S_1 and S_{a1} are notably reduced compared to those in a hard-switching BDC.

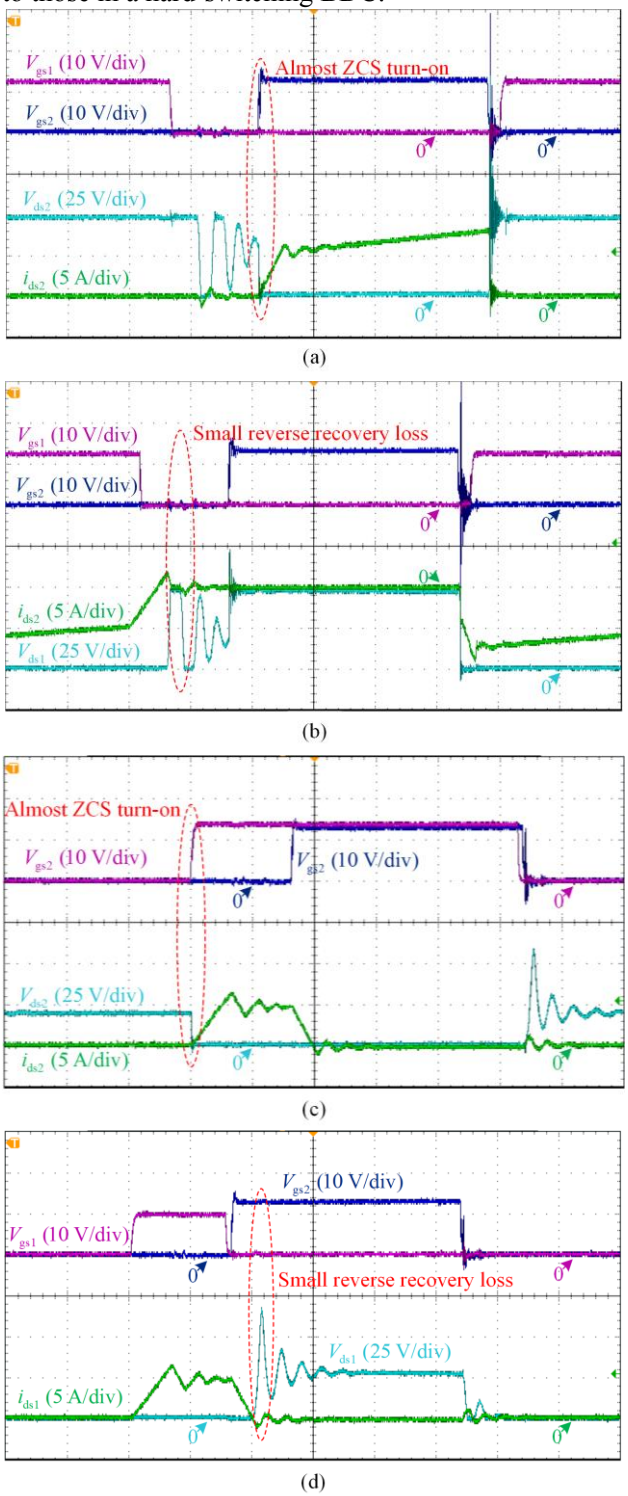


Fig. 11. Switching waveforms in boost mode. (a) Almost ZCS of S_2. (b) Small reverse recovery losses during S_1 turn-off process. (c) Almost ZCS of S_{a2}. (d) Small reverse recovery losses during S_{a1} turn-off process.

B. Inductor Current Ripples Suppression

The experimental results for the inductor current i_L in both buck and boost modes of the BDC with tri-state modulation, compared to a typical soft-switching BDC, are shown in Figs. 12 and 13, respectively.

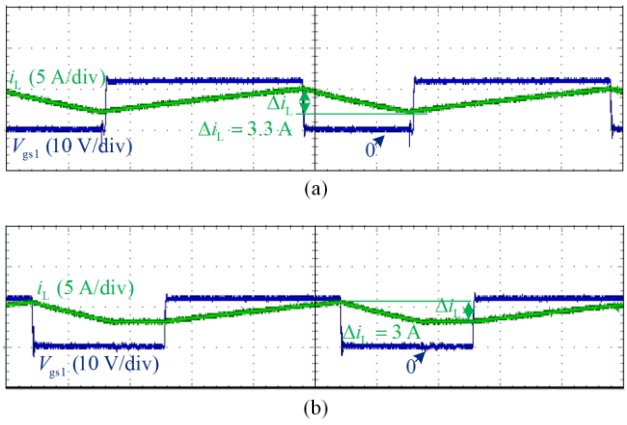


Fig. 12. Inductor current waveforms in buck mode. (a) Typical soft-switching BDC. (b) BDC with tri-state modulation.

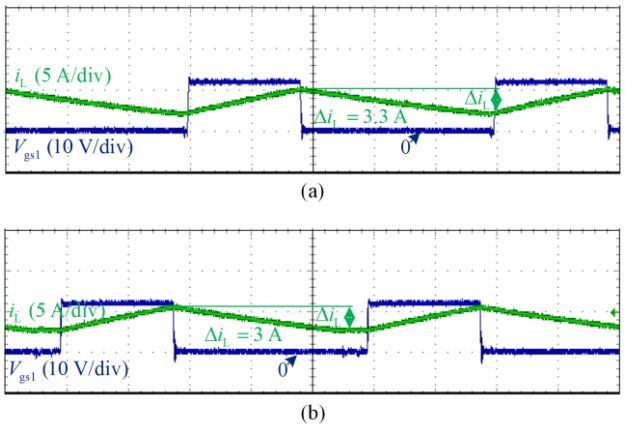


Fig. 13. Inductor current waveforms in boost mode. (a) Typical soft-switching BDC. (b) BDC with tri-state modulation.

The Figs. 12 and 13 illustrate that the inductor current ripple is reduced from 3.3 A in the soft-switching BDC to 3 A in the BDC with tri-state modulation for both modes. Additionally, the average inductor current in the BDC with tri-state modulation increases by approximately 0.65 A compared to that of the typical soft-switching BDC.

C. Minimum Losses Achieving

The efficiency curves for the hard-switching BDC, typical soft-switching BDC, and tri-state modulated BDC, operating under load variations from 45 W to 200 W, are depicted in Fig. 14. Across these three BDCs, the switches, inductance, and switching period are kept constant. As shown, the typical soft-switching BDC demonstrates significantly higher efficiency than the hard-switching BDC over a broad range of loads, except under light loads, the hard-switching BDC operates in discontinuous conduction mode (DCM), where switching losses are minimal, and the primary losses are core. In contrast, for the typical soft-switching BDC, switching losses outweigh the reduction in core losses. The introduction of tri-state modulation allows the BDC to achieve the highest efficiency across a wide load range, reaching a peak efficiency of 96% at 114 W. Furthermore, the efficiency improvement reaches up to 1.7% in buck mode at $P_o = 40$ W compared to the typical soft-switching BDC.

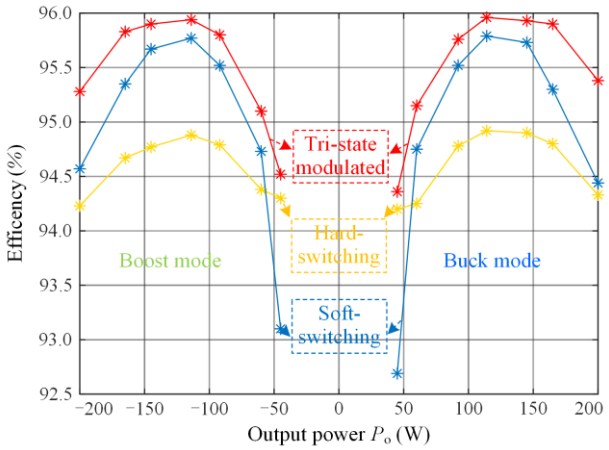


Fig. 14. Measured efficiency in buck and boost modes.

Additionally, Table III presents a comparison of losses, inductor current ripples, and soft-switching conditions among the hard-switching BDC, typical soft-switching BDC, and tri-state modulated BDC. Calculations based on the data show total losses of approximately 11.2 W, 9.08 W, and 8.63 W for hard-switching, typical soft-switching, and tri-state modulated BDCs, respectively. Furthermore, the inductor current ripples for these BDCs are around 3.3 A, 3.3 A, and 3 A, respectively. These results demonstrate that the tri-state modulated BDC significantly reduces inductor current ripples and enhances efficiency.

TABLE III
PERFORMANCE COMPARISON OF THE THREE BDCS

	BDC with tri-state modulation	Hard-switching BDC	Soft-switching BDC
Switching losses	Eq. (31) + Eq. (32) + Eq. (33)	$\frac{1}{2}f(u_H I_L(t_{on}+t_f)+u_H I_L(I_L+I_n)t_{rr})$	Eq. (32) + Eq. (33)
Conduction losses	Eq. (28) + Eq. (29) + Eq. (30)	Eq. (28) + Eq. (29)	Eq. (28) + Eq. (29) + Eq. (30)
Core losses	Eq. (37)	Eq. (37)	Eq. (37)
inductor current ripples	$\frac{(u_H-u_L)}{2Lf}d_c$	$\frac{(u_H-u_L)}{2Lf}d_c$	$\frac{(u_H-u_L)}{2Lf}d_c$
Soft-switching condition	Almost ZCS for S_1 and S_{a1}; ZVS for S_{a2}	Hard-switching for all switches	ZVS for S_1; ZCS for S_{a1}; ZVS for S_{a2}

Note: In hard-switching BDC and soft-switching BDC, d_f equals zero.

Figure 15 illustrates the inductor current ripple in buck mode under different power levels, confirming these findings. While the current ripples for the typical soft-switching BDC remain nearly constant across power levels, tri-state modulated BDC shows a decrease in the current ripple with decreasing power. At 90 W, the ripple reduces to 2.5 A, and at 45 W, it further decreases to 2 A, highlighting a significant reduction compared to the hard-switching and typical soft-switching BDCs. This ripple reduction leads to improved efficiency over a broad power range.

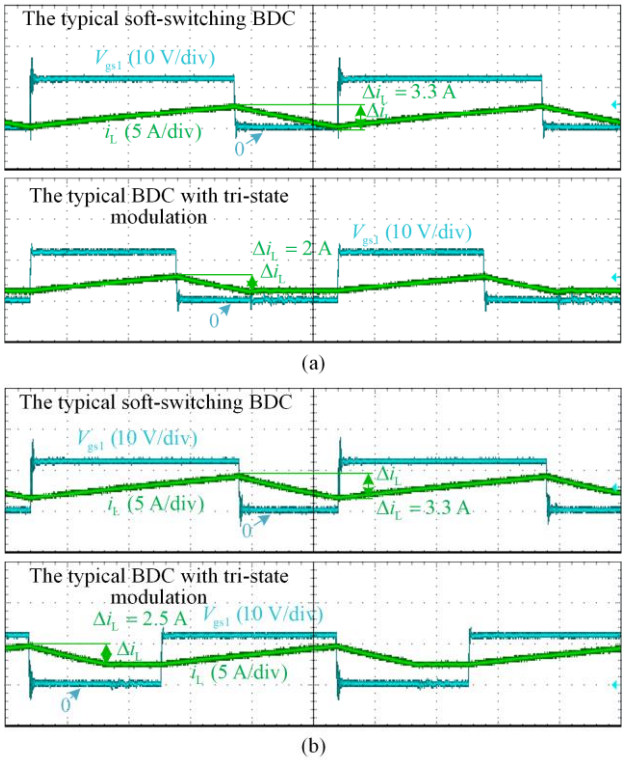
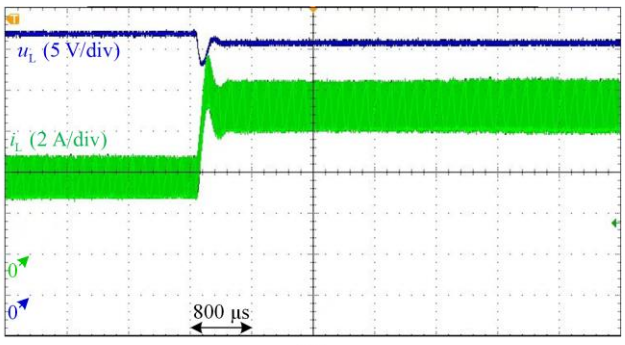


Fig. 15. Inductor current ripple comparison under different power in buck mode. (a) $P = 45$ W. (b) $P = 90$ W.

To analyze the response speed and dynamic characteristics, a dynamic experiment is conducted where the load changed from 90 W to 180 W and the back again. The results illustrated in Fig. 16 show that the overshoot of u_L (blue line) is approximately 9.7%, with a response time of 400 μs in both load-changing situations. Additionally, the overshoot of i_L (green line) is about 28.6% with a response time 400 μs in both cases.



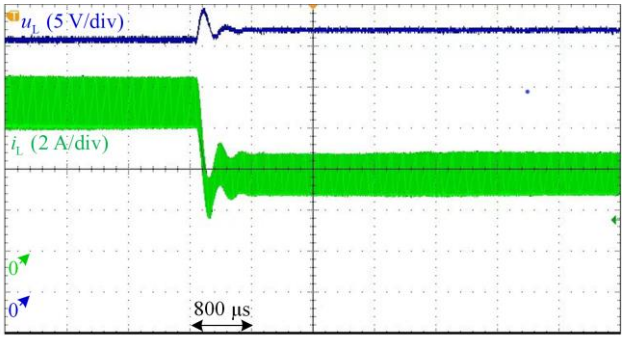


Fig. 16. Dynamic response with load changing. (a) Load changing from 90 W to 180 W. (b) Load changing from 180 W to 90 W.

V. Conclusions

In this paper, a tri-state modulation technique aimed at minimizing operating losses is proposed for a typical soft-switching BDC. This modulation introduces an additional freewheeling interval without altering the original soft-switching characteristics. The inclusion of this freewheeling interval reduces the rise and fall times of the inductor current, effectively suppressing inductor current ripples. Moreover, by appropriately adjusting the freewheeling interval according to load conditions, loss minimization is achieved. The proposed tri-state modulation has been experimentally validated, and the results demonstrate that the tri-state modulated BDC exhibits higher efficiencycompared to a conventional soft-switching BDC, with an efficiency improvement of up to 1.7% under light-load conditions.

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Authors' Contributions

Jiaqi Yu: proposed tri-state modulated BDC, and drafted the original manuscript. Yong Li: wrote the original draft of the manuscript, and in charge of project management. Jianghu Wan: analyzed the topology and wrote the original draft of the manuscript. Feng Zhou: investigated the background and revised English expression. Mingmin Zhang: performed experiment and validated the results. Lihua Cao: checked and revised English expression. All authors read and approved the final manuscript.

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Availability of Data and Materials

Please contact the corresponding author for data material request.

DECLARATIONS

Competing interests: The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this article.

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