Solid-state Circuit Breaker Based on Cascaded Normally-on SiC JFETs for Medium-voltage DC Distribution Networks

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***Abstract*—Solid-state circuit breakers (SSCBs) are critical components in the protection of medium-voltage DC distribution networks to facilitate arc-free, fast and reliable isolation of DC faults. However, limited by the capacity of a single semiconductor device, using semiconductor-based SSCBs at high voltage is challenging. This study presents the details of a 1.5 kV, 63 A medium-voltage SSCB, composed primarily of a solid-state switch based on three cascaded normally-on silicon carbide (SiC) junction field-effect transistors (JFETs) and a low-cost programmable gate drive circuit. Dynamic and static voltage sharing among the cascaded SiC JFETs of the SSCB during fault isolation is realized using the proposed gate drive circuit. The selection conditions for the key parameters of the SSCB gate driver are also analyzed. Additionally, an improved pulse-width modulation current-limiting protection solution is proposed to identify the permanent overcurrent and transient inrush current associated with capacitive load startup in a DC distribution network. Using the developed SSCB prototype and the fault test system, experimental results are obtained to validate the fault response performance of the SSCB.**

***Index Terms*—Solid-state circuit breaker, DC distribution network, SiC JFET, voltage balancing, inrush current.**

I. Introduction

The rapid development of power semiconductor devices and distributed power-generation technologies [1] has led to significant interest in DC power distribution in both academic and industrial circles [2], [3]. However, DC distribution networks have low-impedance characteristics with large DC-link capacitors. Consequently, when a DC short-circuit fault occurs, the peak value of the fault current can be very high, with no natural zero crossing [4]. Thus, further research and development of DC circuit breakers with rapid response are key to the promotion of applications for DC distribution.

Solid-state circuit breakers (SSCBs) that use power semiconductor devices as breaking elements have attracted significant research attention because of their advantages, including fast response, flexible controllability, and arc-free switching [5]–[7]. Recently, numerous novel wide-bandgap (WBG) semiconductor devices have been developed, such as silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs), SiC junction field-effect transistors (JFETs), and SiC static induction transistors (SITs). These SiC power devices have small ON-state resistance, wide safe operating area, and fast switching speed [8–10]. Thus, they are excellent candidates for the development of fast-response SSCBs [11]–[16]. In [11], a low-voltage 400 V SSCB based on SiC SITs is used in a DC distribution system. It effectively reduces the overvoltage of the circuit breaker during fault isolation. Reference [12] develops an 850 V, 100 A circuit breaker using a hybrid power module composed of 1200 V SiC MOSFETs, SiC Schottky diodes, and SiC avalanche breakdown diodes, while in [13], a bidirectional 600 V, 60 A SSCB is proposed using SiC JFETs as static switches. A suitable gate drive circuit for normally-on SiC JFETs is designed to realize DC short-circuit fault protection within a few microseconds [14]. In our previous studies, ultrafast self-powered SSCBs based on normally-on SiC JFETs were reported in [15], [16]. These SSCBs are easy to install as traditional AC air circuit breakers, and the response time is within 10 μs. However, the aforementioned SSCB solutions focus primarily on low-voltage applications ranging from 400 V to 1000 V, but do not meet the requirements for high and medium voltage levels.

Considering the technological limitations of SiC power devices, the nominal voltage of a single commercial SiC device produced by companies such as Infineon, Cree, and UnitedSiC is primarily limited to 1200 V. To increase the voltage level of SiC-based SSCBs, the SiC

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devices in the main static switches must be connected in series to increase their operational voltage levels [17]. When SiC devices are operated in series, influencing factors such as device parameter differences, drive-signal delay, and asymmetry in circuit design can cause unbalanced voltage distribution, which can significantly hinder the safe operation of the SiC devices. Therefore, the dynamic and static voltage balance in series-connected SiC devices is an important issue that must be addressed.

For the voltage balance problem caused by the series arrangement of SiC devices, single-gate drive circuit methods have been proposed to control the turn-on and turn-off states of cascaded SiC devices [18] –[21]. Reference [18] proposes a voltage-balancing method for a super cascade based on 1200 V SiC JFETs and a low-voltage Si MOSFET. This achieves static and dynamic voltage balancing using single MOSFET gate control and an auxiliary circuit. In [19], a voltage balance control method for SiC MOSFET series circuits is presented, in which only the gate of the bottom SiC MOSFET in the series devices is controlled by the circuit, whereas the remaining SiC MOSFETs are controlled using an external power source and an auxiliary circuit. However, the use of a power supply significantly increases the volume and losses of the control system. In [20], a gate-control method suitable for SiC MOSFET series operation based on a snubber circuit is proposed. However, the static voltage balancing needs further improvement. In terms of series connection of normally-on SiC JFETs, reference [21] uses a Zener diode and an *RC* circuit to achieve voltage balancing during SiC JFET cascade operation, thereby increasing the operational voltage of the SSCB. However, this method causes a proportional increase in the number of Zener diodes when the number of series devices increases, which significantly increases the circuit loss. Furthermore, the SSCB only responds to faults with fault current being 4 times or more of the SiC JFET nominal current. In this case, such a high overcurrent is likely to damage the main SiC JFET switches because of overheating. A single-gate driver-cascaded SiC JFETs with an active clamp circuit for a medium-voltage SSCB is proposed in [22], [23]. The complexity of the gate drive circuit is reduced, and the voltage overshoots of the SiC JFETs in series are effectively reduced during SSCB operation. However, more passive components have to be used in this method, and the losses of the drive circuit increase with the increase of the SiC JFETs. Also, the impact of the inrush current generated on the SSCB during capacitive load startup is not considered. Therefore, for a SiC-based SSCB to meet the requirements of medium-voltage operation, a gate drive circuit is necessary to achieve a reliable voltage balance for the SiC series circuit to isolate DC faults quickly and reliably. A cascaded SiC-based SSCB using a simple voltage balancing method and an effective protection strategy is a reasonable option for medium-voltage DC protection.

Previously, we have presented a novel medium-voltage SiC-based SSCB method based on this concept [24]. In this study, the gate drive circuit of the SSCB is further optimized and the operating principles, parameter design considerations, protection schemes, and experimental results of a medium-voltage DC SSCB based on cascading normally-on SiC JFETs are discussed. The main contributions of this paper are:

1) A new voltage-balanced gate drive circuit for medium-voltage SSCB is proposed based on three cascaded normally-on SiC JFETs using the principle of capacitive coupling. This method only requires an external drive signal for the bottom SiC JFET in a series circuit to control the turn-on and turn-off of the SSCB. Thus, improved dynamic and static voltage balancing can be achieved during fault isolation.

2) An improved pulse-width modulation (PWM) current-limiting protection scheme for the SSCB is presented to identify short circuits (4 times or more of the SiC JFET nominal current), overcurrent (2 or 3 times of the SiC JFET nominal current), and inrush current (generated by capacitive loading), which ensures high-quality and reliable operation of the DC distribution network. In addition, during overcurrent protection, the thermal stress of the SiC JFETs in the SSCB main switch is significantly reduced.

The remainder of this paper is organized as follows: Section II presents the operational principles of the novel voltage-balanced circuit for the medium-voltage SSCB, while Section III discusses the selection criteria for the key parameters in the SSCB gate drive circuit obtained via analysis and derivation of the circuit. Section IV demonstrates the improved PWM current-limiting protection scheme for achieving fast DC short circuit and overcurrent fault protection. In Section V, the experimental evaluation of the new SSCB design method is presented, and Section VI presents the main conclusions of the paper.

II. Proposed SSCB Based on Cascaded SIC JFETs

A. Structure and Principle of SSCB

In this study, by exploiting the advantages of normally-on SiC JFET devices, a programmable gate drive circuit of cascaded SiC JFETs is proposed for SSCB, as shown in Fig. 1. In the SSCB, the current and voltage sampling circuits transmit the current i_d flowing through the drain of the SiC JFETs and the load-side voltage V_o to the microprocessor. The two sampled i_d and V_o signals can be used to determine whether short-circuit or overcurrent faults occur in the medium-voltage DC system using a programmable gate-drive circuit, in combination with a fault-protection method.

Finally, the SSCB protects according to the type of DC fault to achieve rapid fault isolation. The DC bus serves as a working power supply directly for the drive circuit using a step-down isolated DC/DC converter, thus eliminating the need for an additional auxiliary power supply and reducing the size of the SSCB. The basic structure and operating principles of the SSCB are described in the following sections.

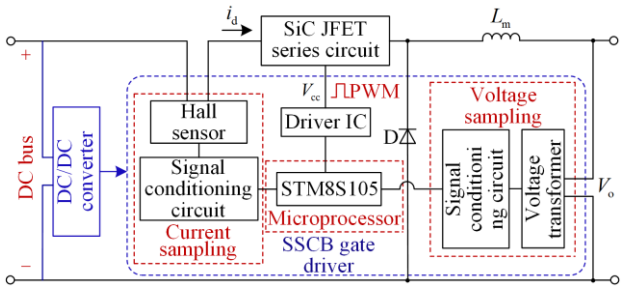


Fig. 1. Simplified schematic diagram of the proposed SSCB.

1) Signal Sampling Circuit

This circuit is composed primarily of current- and voltage-sampling circuits. In the case of a short circuit or an overcurrent fault, i_d flows through the drain of the series-connected SiC JFETs in the SSCB. At this point, the current-sampling circuit uses a fast-response Hall sensor to transmit i_d to the signal-conditioning circuit for processing, and its current value determines the turn-on and turn-off states of the SSCB. When capacitive loading occurs in a DC distribution network, an inrush current is generated, so the SSCB must effectively identify permanent overcurrent faults and inrush current to prevent maloperation. In the voltage-sampling circuit, a voltage transformer is used to detect the load-side voltage V_o. This voltage signal is processed by a signal-conditioning circuit and is then transmitted to the microprocessor. This is the basis for distinguishing between the overcurrent and inrush current to improve protection reliability.

2) Microprocessor Control Unit

The selected microprocessor (STM8S105) in this study is chosen as a compromise between its cost and the data-handling capacity of the fault signals. Combined with the proposed PWM current-limiting protection method, the microprocessor can quickly process the voltage and current signals of the sampling circuit to identify overcurrent and short-circuit faults. Based on the different fault types, a drive control signal is applied to the gate of the SiC JFETs to isolate the faults. Compared with the SSCB and the fault protection methods proposed in [15], the use of the microprocessor facilitates the reliable identification of overcurrents and inrush currents in DC systems. Further, improved efficacy of the SSCB can be realized by designing corresponding protection methods based on the different fault types.

3) SiC JFET Series Circuit

The SiC JFET series circuit is composed primarily of three normally-on SiC JFETs (J_1, J_2, and J_3) connected in series, as shown in Fig. 2. To reduce the influence of the gate drive signal delay or the drive resistance difference on the voltage balance of the cascaded SiC JFETs, a standard gate drive circuit is designed to control the turn-on and turn-off of all the SiC JFETs. In addition, an *RC* voltage snubber circuit is connected in parallel between the drain and source of each SiC JFET to achieve dynamic voltage balance of the SiC JFETs, while resistors R_1, R_2, and R_3 are used to improve the static voltage sharing of the SiC JFETs. Assuming that the microprocessor recognizes a short circuit in the DC network, it sends a trigger signal $V_{cc}(-15\text{ V})$ to the bottom device J_1. At this time, J_1 is turned off and its drain-source voltage gradually increases. When the gate-source voltage of J_2 reaches the clamping voltage V_{cc} of diode D_1 during fast charging of capacitor C_1, J_2 is turned off. Similarly, during the turn-off transient of J_2, the circuit composed of capacitor C_2, resistor R_{g3}, and diode D_2 triggers J_3 to the turn-off state. Thus, the three cascaded SiC JFET devices are turned off individually, and short-circuit fault isolation is realized. In the following sections, the turn-off and turn-on processes of an SSCB based on cascaded SiC JFETs are described in detail.

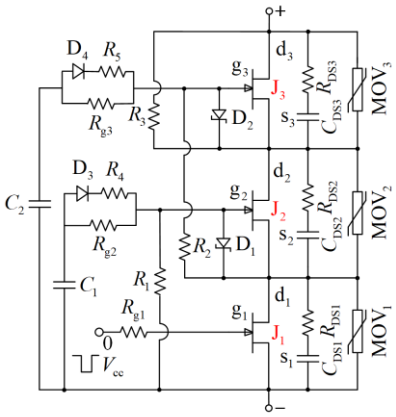


Fig. 2. Structure diagram of the proposed SiC JFET series circuit.

B. Analysis of the SSCB Turn-off Process

In the event of a short circuit or overcurrent, the circuit breaker gate driver immediately processes the current signal i_d and voltage signal V_o, and sends a trigger signal $V_{cc}(-15\text{V})$ to the gate of the cascaded SiC JFETs to interrupt the fault current. The typical voltage and current waveforms of the cascaded SiC JFETs when the SSCB is turned off are depicted in Fig. 3, and the corresponding critical currents are illustrated in Fig. 4. At

time t_0, the initial conditions of the DC network are expressed as follows:

$$\begin{cases} V_{\text{gs-J1}}(t_0)=V_{\text{gs-J2}}(t_0)=V_{\text{gs-J3}}(t_0)=0 \\ I_{\text{D-J1}}(t_0)=I_{\text{D-J2}}(t_0)=I_{\text{D-J3}}(t_0)=I_{\text{o}} \\ V_{\text{ds-J1}}(t_0)=V_{\text{ds-J2}}(t_0)=V_{\text{ds-J3}}(t_0)=I_{\text{o}}R_{\text{DS,on}} \end{cases} \tag{1}$$

where $V_{\text{gs-J1}}$, $V_{\text{gs-J2}}$, $V_{\text{gs-J3}}$, $V_{\text{ds-J1}}$, $V_{\text{ds-J2}}$, $V_{\text{ds-J3}}$ are the gate-source voltages and drain-source voltages across J_1, J_2, and J_3 in the SSCB main switch, respectively; $I_{\text{D-J1}}$, $I_{\text{D-J2}}$, and $I_{\text{D-J3}}$ are the drain currents that flow through J_1, J_2, and J_3, respectively; I_{o} represents the load current flowing through the SSCB and the ON-state resistance of the SiC JFETs is defined as $R_{\text{DS,on}}$.

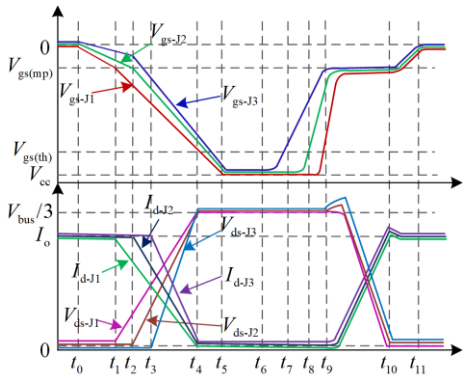


Fig. 3. Idealized voltage and current waveforms of the turn-off and turn-on process for cascaded SiC JFETs.

Stage 1 [t_0-t_1]: assuming that a short circuit occurs at time t_0, the microprocessor generates a drive voltage ($V_{\text{cc}}=-15$ V) to J_1 to enable the SSCB to interrupt the fault current. At this point, V_{cc} charges the gate-source capacitor C_{gs1} via the gate resistor R_{g1}. The charging current i_1 is shown in Fig. 4(a). Subsequently, $V_{\text{gs-J1}}$ gradually increases in the reverse direction from zero. At time t_1, $V_{\text{gs-J1}}(t_1)$ is equal to the Miller plateau voltage $V_{\text{gs(mp)}}$. During this process, $I_{\text{D-J2}}$, $I_{\text{D-J3}}$, $V_{\text{ds-J1}}$, $V_{\text{ds-J2}}$, $V_{\text{ds-J3}}$ are almost constant. The expression for $V_{\text{gs-J1}}(t)$ in this process is given as:

$$V_{\text{gs-J1}}(t)=V_{\text{cc}}(1-\text{e}^{-t/\tau_1}) \tag{2}$$

$$\tau_1=R_{\text{g1}}(C_{\text{gs1}}+C_{\text{gd1}})=R_{\text{g1}}C_{\text{iss1}} \tag{3}$$

where C_{gd1} is the gate-drain capacitor of J_1; C_{iss1} is the equivalent input capacitance of the gate of J_1; and τ_1 is the time constant of $R_{\text{g1}}C_{\text{iss1}}$ circuit. By introducing $V_{\text{gs-J1}}(t_1)=V_{\text{gs(mp)}}$ into (2), the turn-off delay Δt_1 can be obtained as:

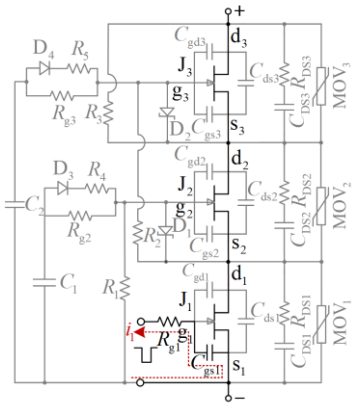
$$\Delta t_1=t_1-t_0=R_{\text{g1}}(C_{\text{gs1}}+C_{\text{gd1}})\ln\left(\frac{-V_{\text{cc}}}{V_{\text{gs(th)}}-V_{\text{cc}}+I_{\text{o}}/g_{\text{m}}}\right) \tag{4}$$

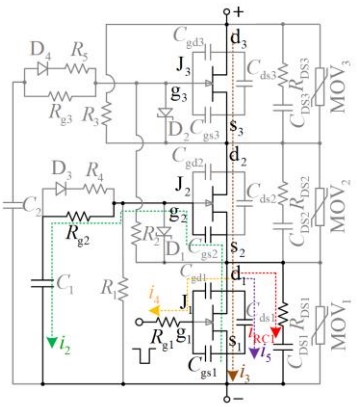
where g_{m} and $V_{\text{gs(th)}}$ are the transconductance and the gate threshold voltage of the SiC JFET, respectively.

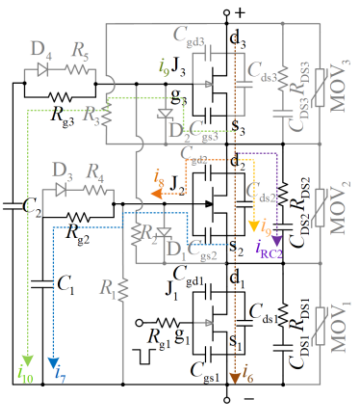
Considering the current-balancing effect in the series circuit, a small leakage current i_5 in the gate circuit of J_2 charges C_1 and C_{gs2} via R_{g2} at this stage, as depicted in Fig. 4(b). Therefore, $I_{\text{D-J1}}$ decreases slowly and $V_{\text{ds-J1}}$ satisfies the following relationship:

$$V_{\text{ds-J1}}=V_{C1}+V_{Rg2}+V_{Cgs2} \tag{5}$$

where V_{C1}, V_{Rg2}, and V_{Cgs2} are the voltages of C_1, R_{g2}, and the gate-source capacitor C_{gs2}, respectively.







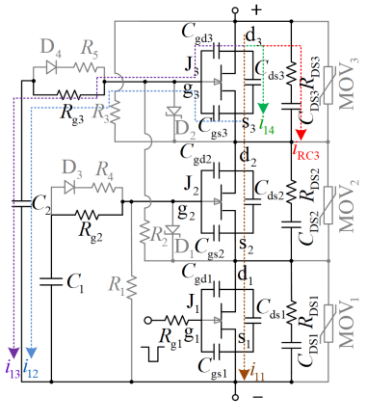


Fig. 4. Main currents of the SiC JFET series circuit during the turn-off process. (a) Stage 1: i_1. (b) Stage 2: i_2, i_3, i_4, i_5 and i_{RC1}. (c) Stage 3: i_6, i_7, i_8, i_9, and i_{RC2}. (d) Stage 4: i_{11}, i_{12}, i_{13}, i_{14}, and i_{RC3}. (e) Stage 5: i_{15}.

Stage 2 [t_1-t_2]: at time t_1, when $V_{\text{gs-J1}}$ is equal to the Miller plateau voltage $V_{\text{gs(mp)}}$, $I_{\text{D-J1}}$ gradually decreases from I_o. At this time, C_{ds1} and C_{gd1} are charged by i_3 and i_4, respectively. $V_{\text{ds-J1}}$ increases further, and its rising rate can be approximated as:

$$\frac{\mathrm{d}V_{\text{ds-J1}}}{\mathrm{d}t} \approx -\frac{i_4}{C_{\text{gd1}}} = \frac{V_{\text{gs-J1}}-V_{\text{cc}}}{R_{\text{g1}}C_{\text{gd1}}} \tag{6}$$

Under the influence of the SiC series circuit, $I_{\text{D-J2}}$ also decreases gradually from I_o. At the same time, the reverse charging process of the gate-source capacitor C_{gs2} of J_2 is accelerated by the increase in $V_{\text{ds-J1}}$, and (5) is still satisfied. Thus, $V_{\text{gs-J2}}$ gradually decreases based on the first stage. The flow paths of the main currents i_2, i_3, i_4, i_5, and i_{RC1} during this stage are shown in Fig. 4(b).

Stage 3 [t_2-t_3]: considering that charging of C_{gs2} has started in the previous stage, $V_{\text{gs-J2}}$ increases from zero to $V_{\text{gs(mp)}}$ at time t_2. At this stage, the increase in $V_{\text{ds-J1}}$ accelerates the charging process of C_{gs2}. According to (6), the rate of increase of $V_{\text{ds-J2}}$ is greater than that of $V_{\text{ds-J1}}$. C_{ds2} and C_{gd2} of J_2 are charged by i_8 and i_9, respectively. The flow paths of i_6, i_7, i_8, i_9, and i_{RC2} are shown in Fig. 4(c).

In addition to the increase in $V_{\text{ds-J2}}$, the voltage of the gate-source capacitor C_{gs3} of J_3 also gradually increases from zero in the reverse direction. Thus, the following relationship can be obtained for the gate circuit of J_3:

$$V_{C2}+V_{Rg3}+V_{Cgs3}=V_{\text{ds-J1}}+V_{\text{ds-J2}} \tag{7}$$

where V_{C2}, V_{Rg3}, and V_{Cgs3} are the voltages associated with C_2, R_{g3}, and the gate-source capacitor C_{gs3}, respectively.

Stage 4 [t_3-t_4]: during the rapid charging of C_{gs3} in Stage 3, $V_{\text{gs-J3}}$ increases to $V_{\text{gs(mp)}}$ at time t_3. Similarly, $V_{\text{ds-J3}}$ further increases owing to the charging of C_{ds3} and C_{gd3} by i_{13} and i_{14}, respectively. At time t_4, $V_{\text{gs-J1}}$, $V_{\text{gs-J2}}$, and $V_{\text{gs-J3}}$ gradually increase to the gate threshold voltage $V_{\text{gs(th)}}$, and the drain currents $I_{\text{D-J1}}$, $I_{\text{D-J2}}$, and $I_{\text{D-J3}}$ decrease to zero. The drain-source voltages $V_{\text{ds-J1}}$, $V_{\text{ds-J2}}$, and $V_{\text{ds-J3}}$ of all the series devices increase to one-third of V_{bus}. The path diagrams for i_{11}, i_{12}, i_{13}, i_{14}, and i_{RC3} at this stage are shown in Fig. 4(d).

Stage 5 [t_4-t_5]: in this stage, $V_{\text{gs-J1}}$, $V_{\text{gs-J2}}$, and $V_{\text{gs-J3}}$ reverse increase from zero to the bias voltage V_{cc}(−15 V). All cascaded devices are in the off state, and the SiC JFETs are completely turned off, there is only a very small leakage current i_{15} flowing through the SSCB as shown in Fig. 4(e). Considering that the equivalent resistances of J_1, J_2, and J_3 are much larger than those of R_1, R_2, and R_3 after they are completely turned off, no leakage current flows through the SiC JFETs. The static voltage balance between the series-connected SiC JFETs in the cutoff state is maintained by R_1, R_2, and R_3, i.e., $V_{\text{ds-J1}}$, $V_{\text{ds-J2}}$, $V_{\text{ds-J3}}$ are one-third of the DC-bus voltage V_{bus}.

C. Analysis of the SSCB Turn-on Process

If a short circuit or an overcurrent in the DC network is completely cleared, the SSCB changes from the off state to the on state. The voltage and current waveforms during the turn-on transition of the cascaded SiC JFETs are shown in Fig. 3, while the corresponding critical currents are shown in Fig. 5. At time t_6, the initial condition of the DC system is assumed to be:

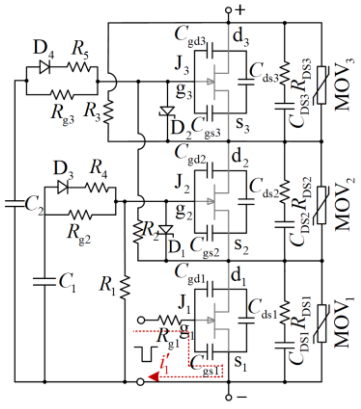
$$\begin{cases} V_{\text{gs-J1}}(t_6)=V_{\text{gs-J2}}(t_6)=V_{\text{gs-J3}}(t_6)=V_{\text{cc}} \\ I_{\text{D-J1}}(t_6)=I_{\text{D-J2}}(t_6)=I_{\text{D-J3}}(t_6)=0 \\ V_{\text{ds-J1}}(t_6)=V_{\text{ds-J2}}(t_6)=V_{\text{ds-J3}}(t_6)=V_{\text{bus}}/3 \end{cases} \tag{8}$$

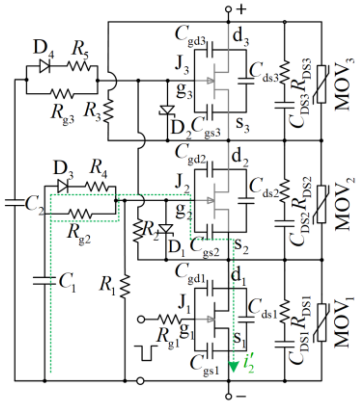
Stage 6 [t_6-t_7]: when the fault in the DC network is cleared, the gate voltage V_{cc} increases from −15 V to 0 V at time t_6, causing the SSCB to turn on. The voltage V_{cc} on the gate-source capacitor C_{gs1} of J_1 is discharged in reverse through R_{g1}, and the discharge current i_1' is depicted in Fig. 5(a). Subsequently, $V_{\text{gs-J1}}$ starts increasing from −15 V and reaches the threshold voltage $V_{\text{gs(th)}}$ at time t_7. During this process, the cascaded devices J_1, J_2, and J_3 are still in the off state. Simultaneously, the gate-source voltages $V_{\text{gs-J2}}$ and $V_{\text{gs-J3}}$ are stable at −15 V, i.e., the drain-source voltages $V_{\text{ds-J1}}$, $V_{\text{ds-J2}}$, and $V_{\text{ds-J3}}$ remain unchanged. The relationship between $V_{\text{gs-J1}}(t)$ and V_{cc} during this process is given as:

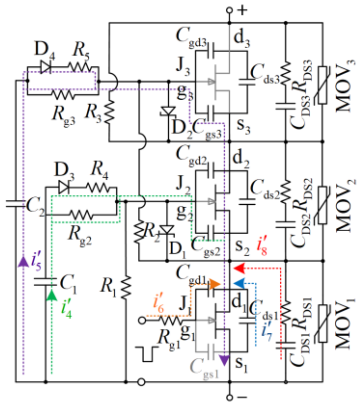
$$V_{\text{gs-J1}}(t)=V_{\text{cc}}\text{e}^{-t/\tau_1} \tag{9}$$

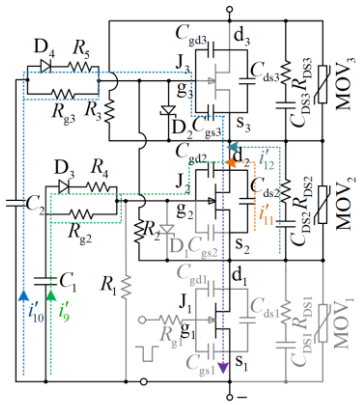
Combining $V_{\text{gs-J1}}(t_7)=V_{\text{gs(th)}}$ with (9), the turn-on delay time Δt_2 is given by:

$$\Delta t_2=t_7-t_6=R_{\text{g1}}(C_{\text{gs1}}+C_{\text{gd1}})\ln\left(\frac{V_{\text{cc}}}{V_{\text{gs(th)}}}\right) \tag{10}$$









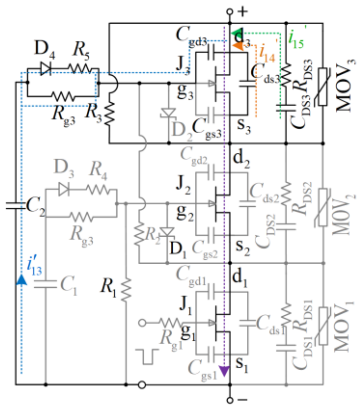


Fig. 5. Main currents of the SiC JFET series circuit during the turn-on process. (a) Stage 6: i_1'. (b) Stage 7: i_2'. (c) Stage 8: i_3'. (d) Stage 9: i_4', i_5', i_6', i_7', and i_8'. (e) Stage 9: i_9', i_{10}', i_{11}', and i_{12}'. (f) Stage 9: i_{13}', i_{14}', and i_{15}'.

Stage 7 [t_7-t_8]: at time t_7, J_1 turns on because its gate-source voltage $V_{\text{gs-J1}}(t_7)$ is equal to $V_{\text{gs(th)}}$. In this stage, with the continuous discharge of C_{gs1}, the drain current i_{d} of a single SiC JFET increases linearly with $V_{\text{gs-J1}}$, and i_{d} can be obtained as:

$$i_{\text{d}}(t)=g_{\text{m}}\left[V_{\text{gs-J1}}(t)-V_{\text{gs(th)}}\right] \tag{11}$$

Under the influence of the turn-on process, J_1, R_4,

D_3, C_1, and C_{gs2} form a discharge loop in the gate circuit of J_2. The series branch composed of resistor R_4 and diode D_3 facilitates the acceleration of the discharge of C_1 and C_{gs2}, thereby promoting the fast turn-on of J_2. The discharge current i_2' is shown in Fig. 5(b) and the following relationship exists:

$$V_{C1}+V_{Rg2}+V_{Cgs2}=V_{ds\text{-}J1} \tag{12}$$

Consequently, the gate-source voltage $V_{gs\text{-}J2}$ of J_2 gradually increases from V_{cc}.

Stage 8 [t_8-t_9]: during this stage, the gate-source voltage $V_{gs\text{-}J2}(t_8)$ of J_2 is equal to $V_{gs(th)}$ at time t_8, J_3 remains in the off state. Therefore, R_5, D_3, and C_2 and C_{gs3} form a discharge loop in the gate circuit of J_3, and the discharge current i_3' is shown in Fig. 5(c). Thus, there is:

$$V_{C2}+V_{Rg3}+V_{Cgs3}=V_{ds\text{-}J1}+V_{ds\text{-}J2} \tag{13}$$

Therefore, the gate-source voltage $V_{gs\text{-}J3}$ gradually increases and reaches the threshold voltage $V_{gs(th)}$ at time t_9.

Stage 9 [t_9-t_{10}]: when $V_{gs\text{-}J3}=V_{gs(th)}$, J_3 is turned on, and $I_{D\text{-}J1}$, $I_{D\text{-}J2}$, and $I_{D\text{-}J3}$ gradually increase from zero. $V_{gs\text{-}J1}$ reaches the Miller plateau voltage $V_{gs(mp)}$ at this stage, and therefore, $V_{ds\text{-}J1}$ gradually decreases from one-third of V_{bus}. C_{gd1}, C_{ds1}, and C_{DS1} begin discharging, and the discharge currents i_4', i_5', i_6', i_7', and i_8' are shown in Fig. 5(d). Owing to the rapid reduction in $V_{ds\text{-}J1}$, C_1 in the gate circuit of J_2 accelerates the discharge of C_{gs2} via R_4 and D_3. Therefore, the following relationship is obtained:

$$\begin{cases}\left[(R_{g2}+R_4)/R_{g2}R_4\right]i_4'+V_{gs\text{-}J2}+V_{ds1}=V_{C1}\\ C_1\dfrac{\mathrm{d}V_{C1}}{\mathrm{d}t}=-C_{gs2}\dfrac{\mathrm{d}V_{gs\text{-}J2}}{\mathrm{d}t}\end{cases} \tag{14}$$

To simplify the calculation, the gate current i_4' of J_2 is considered to be approximately constant, and (14) can be calculated as:

$$\frac{\mathrm{d}V_{gs\text{-}J2}}{\mathrm{d}t}=-\frac{C_1}{C_1+C_{gs2}}\frac{\mathrm{d}V_{ds\text{-}J1}}{\mathrm{d}t} \tag{15}$$

Evidently from (15), with a rapid reduction in $V_{ds\text{-}J1}$, the discharge speed of C_{gs2} increases, and $V_{gs\text{-}J2}$ gradually increases. When $V_{gs\text{-}J2}$ increases to $V_{gs(mp)}$, $V_{ds\text{-}J2}$ reaches its peak value. Thereafter, $V_{ds\text{-}J2}$ decreases rapidly from its maximum value. Simultaneously, C_{gd2}, C_{ds2}, and C_{DS2} begin discharging, and the discharge currents i_9', i_{10}', i_{11}', and i_{12}' are shown in Fig. 5(e).

Similarly, when $V_{ds\text{-}J2}$ decreases rapidly, C_2 in the gate circuit of J_3 accelerates the discharge of C_{gs3} via R_5 and D_4 to yield the following:

$$\begin{cases}\left[(R_{g3}+R_5)/R_{g3}R_5\right]i_{10}'+V_{gs\text{-}J3}+V_{ds\text{-}J2}=V_{C2}\\ C_2\dfrac{\mathrm{d}V_{C2}}{\mathrm{d}t}=-C_{gs3}\dfrac{\mathrm{d}V_{gs\text{-}J3}}{\mathrm{d}t}\end{cases} \tag{16}$$

If the gate current i_{10}' of J_3 is approximated to be constant, the corresponding solution to (16) can be determined by:

$$\frac{\mathrm{d}V_{gs\text{-}J3}}{\mathrm{d}t}=-\frac{C_2}{C_2+C_{gs3}}\left(\frac{\mathrm{d}V_{ds\text{-}J1}}{\mathrm{d}t}+\frac{\mathrm{d}V_{ds\text{-}J2}}{\mathrm{d}t}\right) \tag{17}$$

Based on (17), as $V_{ds\text{-}J1}$ and $V_{ds\text{-}J2}$ decrease, C_{gs3} discharges rapidly, and $V_{gs\text{-}J3}$ gradually increases. Therefore, $V_{ds\text{-}J3}$ reaches its maximum when $V_{gs\text{-}J3}$ is equal to $V_{gs(mp)}$. At this stage, the discharge currents i_{13}', i_{14}', and i_{15}' correspond to C_{gd3}, C_{ds3}, and C_{DS3} respectively, as shown in Fig. 5(f).

Stage 10 [$t_{10}-t_{11}$]: at time t_{10}, J_1, J_2, and J_3 are all turned on. The drain-source voltages $V_{ds\text{-}J1}$, $V_{ds\text{-}J2}$, and $V_{ds\text{-}J3}$ all decrease to zero. During this period, influenced by the driving signal V_{cc}, $V_{gs\text{-}J1}$ further increases from $V_{gs(mp)}$ to zero. After the discharging of C_1 and C_2 is complete, $V_{gs\text{-}J2}$ and $V_{gs\text{-}J3}$ further increase from $V_{gs(mp)}$ to zero. At t_{11}, the SSCB returns to its normal state.

III. Key Parameter Settings of the SSCB Gate Driver

A. Parameter Selection of C_1 and C_2

During the turn-on and turn-off processes of the cascaded SiC JFETs, the bottom device J_1 is driven by a standard single-gate driver, while J_2 and J_3 are driven by the charge transfer between the capacitors in their respective gate circuits. An analysis of the turn-off process for J_2 during Stage 3 is considered as an example. Based on the principle of charge conservation, the following expression is satisfied:

$$C_1\Delta V_{C1}=C_{gs\text{-}J2}\Delta V_{gs\text{-}J2}+C_{gd2}\Delta V_{gd\text{-}J2} \tag{18}$$

where ΔV_{C1} is the voltage variation of C_1; $\Delta V_{gs\text{-}J2}$ and $\Delta V_{gd\text{-}J2}$ are the voltage variations of C_{gs2} and C_{gd2}, respectively. And the following relationship holds:

$$\begin{cases} V_{C1} = V_{\text{ds-J1}} + V_{\text{gs-J2}} + V_{Rg2} \\ V_{\text{gd-J2}} = V_{\text{gs-J2}} - V_{\text{ds-J2}} \end{cases} \tag{19}$$

In general, the gate currents of J_2 and J_3 are small, and $V_{\text{gs-J2}}$ and $V_{\text{gs-J3}}$ are maintained within the V_{cc} range by Zener diodes D_1 and D_2, respectively. Therefore, V_{Rg2}, V_{Rg3}, $V_{\text{gs-J2}}$, and $V_{\text{gs-J3}}$ can be ignored in the approximation. In this case, C_1 and C_2 are approximated as:

$$C_i = \frac{3V_{\text{cc}}C_{\text{gs}(i+1)} + V_{\text{bus}}C_{\text{gd}(i+1)}}{3V_{Ci}}, i = 1,2 \tag{20}$$

According to (19) and (20), the voltage V_{C2} of C_2 is approximately twice that of C_1 in the steady state. Thus, C_1 has the following option:

$$C_1 \approx 2C_2 \tag{21}$$

B. Parameter Selection of R_{g1}, R_{g2} and R_{g3}

In the gate drive circuit of the SSCB, in addition to the parasitic capacitor C_{gs} and gate resistor R_{g} of the SiC JFET, the equivalent inductance L_{eq} includes the printed circuit board (PCB) circuit and the parasitic and stray inductances of the device. Together, these parameters form a multi-order system. To reduce the electrical oscillation in the SiC JFET gate circuit, appropriate gate resistors R_{g1}, R_{g2}, and R_{g3} must be selected to ensure that the corresponding gate circuits operate in an overdamping or critical-damping state. Thus, R_{g1} conforms to the following relationship:

$$R_{\text{g1}} > 2\sqrt{\frac{L_{\text{eq}}}{C_{\text{gs1}}}} \tag{22}$$

Given that C_1 and C_2 accelerate the turn-on and turn-off speeds of J_2 and J_3, the gate resistors R_{g2} and R_{g3} satisfy the following condition:

$$R_{\text{g}(i+1)} > 2\sqrt{\frac{L_{\text{eq}}}{C_{\text{gs}(i+1)} + C_i}}, i = 1,2 \tag{23}$$

The larger the equivalent inductance L_{eq} is, the more significant the oscillation phenomenon appears in the SSCB gate circuit. In the actual PCB design process, if R_{g1}, R_{g2}, and R_{g3} are as close to the gate pins of the corresponding SiC JFETs as possible, the oscillation can be suppressed.

The resistance values of R_{g1}, R_{g2}, and R_{g3} determine the rise and fall times of the SiC JFET gate drive signals. To avoid the increase in power consumption caused by long rise and fall times, the minimum conduction time, $T_{\text{on\_min}}$ of the SiC JFET device can be used to approximately determine the maximum values of R_{g1}, R_{g2}, and R_{g3}. The SiC JFETs used in this study are UJ3N120035K3S, produced by UnitedSiC, and the typical minimum conduction time $T_{\text{on\_min}}$ is approximately 37 ns. Thus, R_{g1}, R_{g2}, and R_{g3} are approximated by:

$$R_{\text{g}i} < \frac{1}{40}\frac{T_{\text{on\_min}}}{C_{\text{gs}i}}, i = 1,2,3 \tag{24}$$

Consequently, to satisfy the requirements of the SSCB for oscillation suppression and rapid response, R_{g1}, R_{g2}, and R_{g3} should be as small as possible within the allowable range. During the SSCB turn-on process, the maximum dynamic voltage imbalance occurs during the turn-on times of J_2 and J_3. Using R_4, R_5, D_3, and D_4, the turn-on speeds of J_2 and J_3 can be further improved, and the dynamic voltage imbalance of the cascaded SiC JFETs is reduced.

C. Influence of Key Parameters on the SSCB

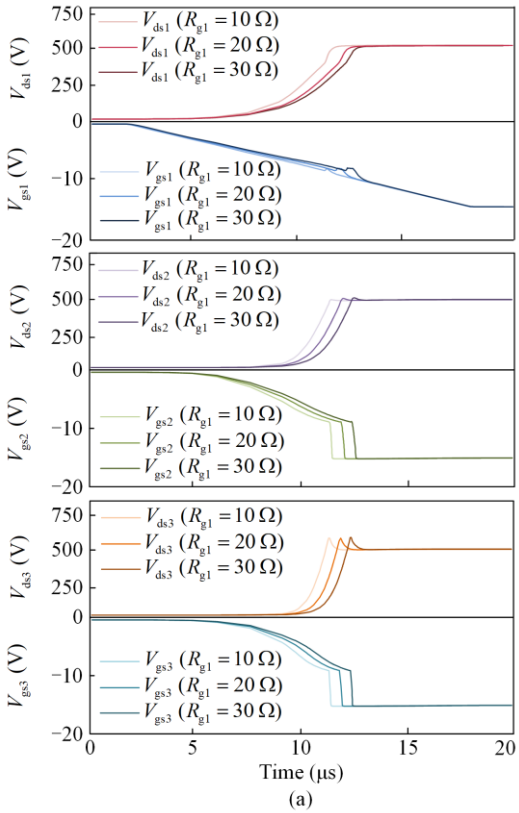
To assess the influence of the gate resistors (R_{g1}, R_{g2}, and R_{g3}) and drive capacitors (C_1 and C_2) on the switching characteristics of the SSCB, a simulation model of the SiC JFET series circuit shown in Fig. 2 is built using ORCAD/PSpice. The main parameters of the series circuit are listed in Table I. Taking the gate resistor R_{g1} and the drive capacitor C_1 as examples, the drain-source voltages $V_{\text{ds1,2,3}}$ and gate-source voltages $V_{\text{gs1,2,3}}$ during the turn-off of the cascaded SiC JFETs are observed when the values of R_{g1} and C_1 are varied. The influence of R_{g1} and C_1 on the voltage balance of the cascaded SiC JFETs is analyzed and the simulation results are presented in Fig. 6.

TABLE I
MAIN COMPONENT PARAMETERS IN THE SIMULATION

Parameters	Values
Gate resistor R_{g1}	10 Ω
Gate resistor R_{g2}, R_{g2}	5 Ω
Gate discharge resistor R_4, R_5	0.2 Ω
Gate capacitor C_1	500 pF
Gate capacitor C_2	200 pF
Snubber capacitors C_{DS1}, C_{DS2}, C_{DS3}	2.2 nF
Snubber capacitors R_{DS1}, R_{DS2}, R_{DS3}	200 Ω
Voltage balancing resistor R_1, R_2, R_3	100 kΩ
SiC JFET (UJ3N120035K3S UnitedSiC)	1.2 kV/63 A
Limit current inductance L_{m}	0.028 mH
DC-bus voltage V_{bus}	1.5 kV
Cable π-equivalent resistance R_x	120 mΩ/km
Cable π-equivalent inductance L_x	0.56 mH/km
DC-link capacitor C_{link}	5 mF

When R_{g1} is adjusted, R_{g2}, R_{g3}, C_1, and C_2 remain unchanged. The operating conditions for the voltages

$V_{ds1,2,3}$ and $V_{gs1,2,3}$ are shown in Fig. 6(a). The results indicate that when R_{g1} increases from 10 Ω to 30 Ω, the decrease rate of $V_{gs1,2,3}$ from 0 to −15 V reduces, and the turn-off times of J_1, J_2, and J_3 are prolonged. However, the drain-source voltages $V_{ds1,2,3}$ of J_1, J_2, and J_3 are maintained at 500 V after the device is completely turned off. When C_1 increases from 100 pF to 500 pF, R_{g1}, R_{g2}, R_{g3}, and C_2 remain unchanged. The voltages $V_{ds1,2,3}$ and $V_{gs1,2,3}$ of the cascaded SiC JFETs vary with C_1, as shown in Fig. 6(b). The simulation results show that the increase in C_1 increases the charging speed of the gate-source capacitor $C_{gs\text{-}J2}$, and this causes V_{gs2} to decrease rapidly. This results in a shorter time for V_{ds2} to increase from 0 to 500 V. Simultaneously, during the charging effect of V_{ds2} on $C_{gs\text{-}J3}$, the turn-off speed of J_3 is also improved. However, V_{gs1} is not affected by C_1, thus causing V_{ds1} to be less than 500 V when the cascade SiC JFETs are turned off. Therefore, variation in C_1 has a significant influence on the voltage balance of the cascaded SiC JFETs. These results of the simulation analyses can serve as a reference for the selection of important SSCB parameters.



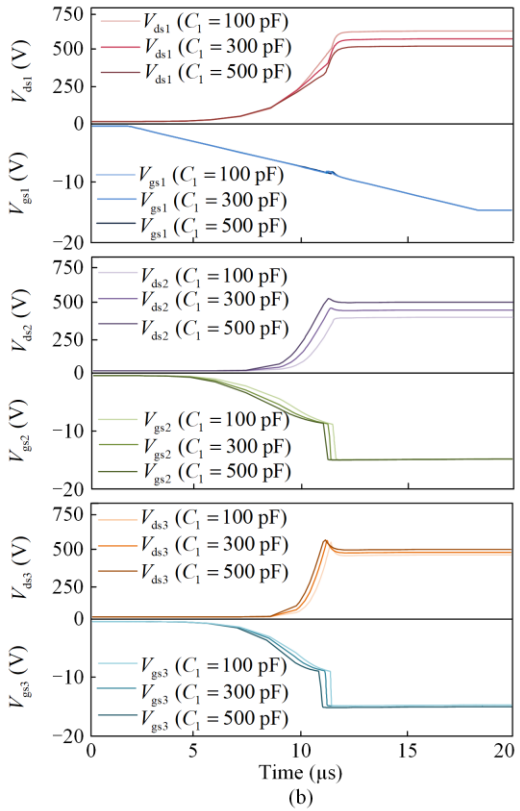


Fig. 6. Simulation results of the SiC JFET series circuit when the values of R_{g1} and C_1 are varied respectively. (a) $V_{DS1,2,3}$ and $V_{gs1,2,3}$ results for a set of different values of R_{g1}. (b) $V_{DS1,2,3}$ and $V_{gs1,2,3}$ results for a set of different capacitances of C_1.

IV. Current Limiting Protection Method for SSCB

A. Protection Principle of the SSCB

When a fault occurs in a DC distribution network as shown in Fig. 7, the increasing rate and amplitude of the fault current depend primarily on the fault type. Therefore, to better distinguish between the fault types and prevent maloperation of the SSCB, protection is provided according to the fault situation. A flowchart of the SSCB protection method is presented in Fig. 8. The implementation process of the SSCB protection is described in the following sections.

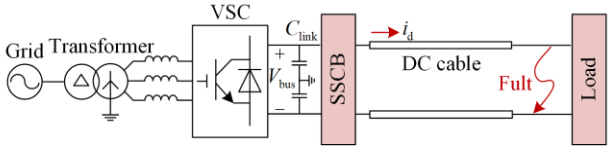


Fig. 7. Schematic of a DC distribution network with the proposed SSCB.

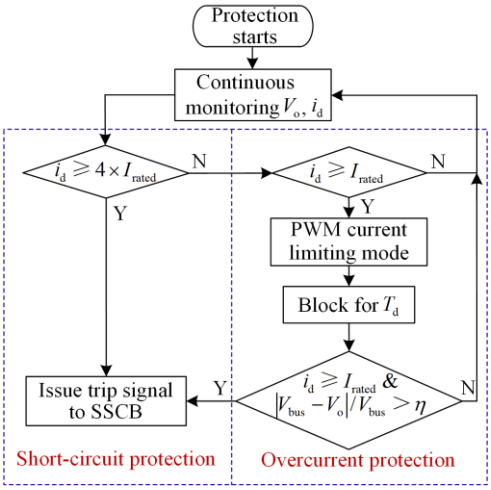


Fig. 8. Flowchart of the current limiting protection method for SSCB.

1) Normal Operation

When the current i_d monitored by the SSCB current-sampling circuit satisfies $i_d \leq I_{rated}$ (I_{rated} is the SiC JFET nominal current), the SiC JFET series circuit of the SSCB is maintained in the on state, and the DC system operates normally.

2) Short-circuit Protection

Generally, short circuits are serious types of faults in DC systems. After a short-circuit fault occurs, the SSCB must isolate the fault before i_d increases to an unacceptable value. Considering the safety of the SiC JFET device, when i_d is greater than or equal to $4I_{rated}$, it can be regarded as a short circuit. Here, the microprocessor applies −15 V to the gate of J_1, thus causing the SSCB to turn off.

3) Overcurrent Protection

When i_d is such that $I_{rated} < i_d < 4I_{rated}$, an overcurrent event occurs in the DC system. The junction temperature of SiC JFETs continues to increase after a long period of overcurrent. This can cause thermal damage to the SiC JFETs. However, the short-term inrush current generated by capacitive load startup has a minor impact on the safe operation of the DC network, and the SSCB must be maintained in the on state. In this case, the SSCB can prevent maloperation by distinguishing between the overcurrent and the inrush current, thus enhancing the reliability of the SSCB. Therefore, when the SSCB detects that i_d satisfies $I_{rated} < i_d < 4I_{rated}$, it adopts a PWM current-limiting mode with the delay time T_d. This mode is used to limit the time that the SSCB is in an overcurrent state, thereby reducing the thermal stress of the SiC JFETs. The delay time T_d can be selected according to the maximum thermal capacity of the SiC JFET for different overcurrent values. Reference [16] has already discussed the relevant theoretical basis for setting T_d in detail, and thus it is not elaborated further here. Consequently, the SSCB adopts different protection principles for the aforementioned two overcurrent conditions.

1) Overcurrent fault: if $I_{rated} < i_d < 4I_{rated}$, a PWM control signal is applied to the gate of the cascaded SiC JFETs. After a period of T_d, $I_{rated} < i_d < 4I_{rated}$ is still satisfied, while the load voltage V_o cannot be restored to the normal level $|V_{bus}-V_o|/V_{bus} > \eta$ (in this study, η is set to 10%). Thus, the occurrence of a permanent overcurrent fault in the DC system can be deduced. At this time, the microprocessor sends a negative gate signal V_{cc} to the gate of J_1 to turn-off the SSCB.

2) Inrush current: after the SSCB experiences a T_d period in the PWM mode, i_d returns to the normal level ($i_d \leq I_{rated}$), and the load voltage V_o satisfies the condition $|V_{bus}-V_o|/V_{bus} \leq \eta$. i_d is considered to be an inrush current generated during capacitive load startup, and therefore the SSCB returns to its normal on state.

B. Simulation Results for SSCB

The simulation model corresponding to Fig. 7 is developed in PSCAD/EMTDC to evaluate the effectiveness of the proposed SSCB protection method for different DC fault types, while the system parameters were presented in Table I. The SSCB simulation waveforms when the short-circuit fault, overcurrent, and inrush current occurred are shown in Fig. 9.

The simulation results of the DC-bus voltage V_{bus}, drain-source voltage V_{DS} and drain current i_d of the SSCB during the short-circuit fault are shown in Fig. 9(a). As seen, at 0.9 ms, i_d is increased sharply after the short-circuit fault. When i_d reaches 4 times the SiC JFET nominal current, the SSCB responds to the short-circuit fault and finally completes fault isolation. As shown in Fig. 9(b), when a permanent overcurrent fault occurs in the DC system at 0.9 ms, i_d increases rapidly from 25 A to approximately 130 A. To determine whether i_d is a permanent overcurrent, the SSCB enters into the PWM current-limiting mode with a delay time of 1.8 ms. At the end of the current limiting mode, i_d is still greater than the SiC JFET nominal current (63 A) while V_o satisfies the inequality $|V_{bus}-V_o|/V_{bus} > 10\%$. At this time, to prevent thermal damage to the SiC JFETs owing to the continuous overcurrent, the SSCB is turned off, and overcurrent protection is achieved. Fig. 9(c) shows the waveforms for the SSCB when an inrush current is generated by the capacitive load. Evidently, when the DC system operates normally, i_d is 25 A. At 0.9 ms, capacitive loading occurs in the DC system, and i_d increases rapidly from 25 A to approximately 125 A. In this case, the SSCB also enters into PWM current-limiting mode. After

a delay time T_d of 1.8 ms, i_d is less than the rated current of 63 A, while V_o satisfies the inequality $|V_{bus}-V_o|/V_{bus}\leqslant 10\%$. The SSCB is then switched to the on state.

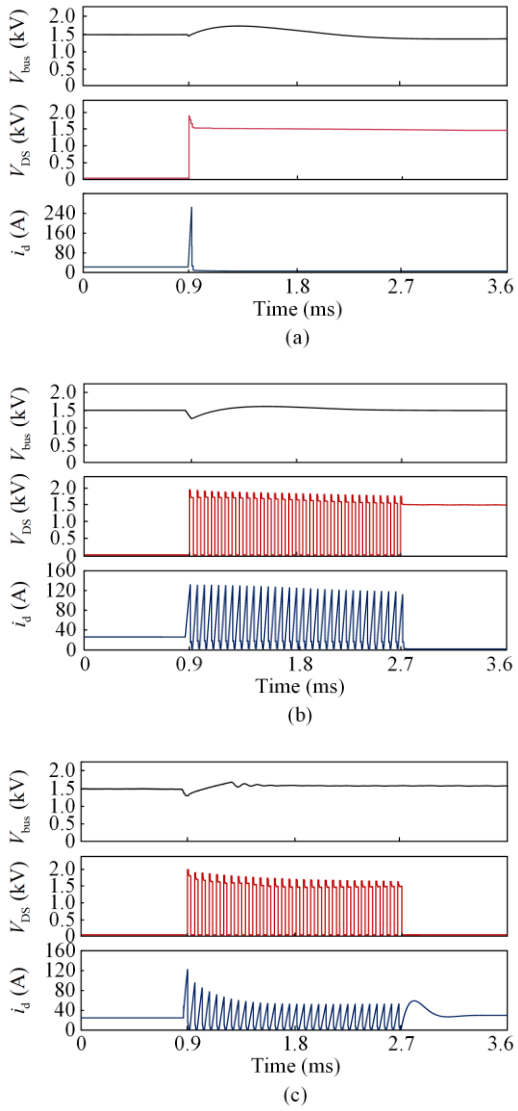


Fig. 9. Simulation waveforms of the SSCB when short-circuit fault, overcurrent, and inrush current occurred. (a) V_{bus}, V_{DS}, and i_d results for a short-circuit fault. (b) V_{bus}, V_{DS}, and i_d results for an overcurrent. (c) V_{bus}, V_{DS}, and i_d results for an inrush current.

V. Experimental Results

As shown in Fig. 10(a), to experimentally evaluate the effectiveness of the proposed topology, a 1.5 kV, 63 A SSCB prototype based on three cascaded normally-on SiC JFETs has been developed. Figs. 11 and 10(b) show the simplified schematic and image of the fault test set-up, respectively. Tests are performed at a maximum DC voltage of 750 V, and the key parameters of the SSCB prototype and the test set-up are listed in Table II.

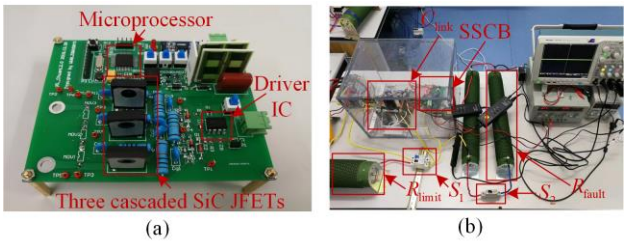


Fig. 10. Image of the designed SSCB prototype and DC fault test set-up. (a) SSCB prototype. (b) Test set-up.

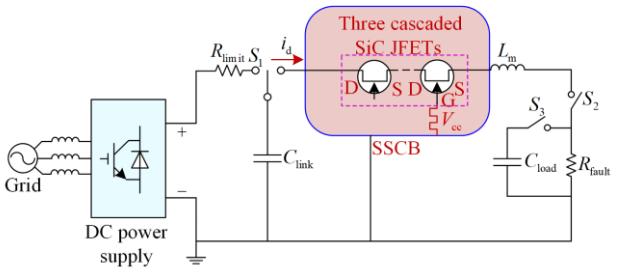


Fig. 11. Simplified schematic of DC fault test set-up.

TABLE II
Electrical Parameters of the SSCB Prototype and the Test Set-up

Parameters	Values
Gate resistor R_{g1}	10 Ω
Gate resistor R_{g2}, R_{g3}	5 Ω
Gate discharge resistor R_4, R_5	0.2 Ω
Gate capacitor C_1	470 pF
Gate capacitor C_2	220 pF
Snubber capacitors C_{DS1}, C_{DS2}, C_{DS3}	2.2 nF
Snubber capacitors R_{DS1}, R_{DS2}, R_{DS3}	200 Ω
Voltage balancing resistor R_1, R_2, R_3	100 kΩ
Microprocessor	STM8S105
SiC JFET (UJ3N120035K3S UnitedSiC)	1.2 kV/63 A
DC-link capacitor C_{link}	2.2 mF
Load capacitor of test setup C_{load}	100 μF
Limit resistor of test setup R_{limit}	100 Ω
Limit current inductance L_m	0.028 mH

A. Short-circuit Experimental Results

In the test set-up, switch S_1 is used to connect the DC-link capacitor C_{link} to the DC power supply to charge the voltage V_{bus} of C_{link} to 750 V. Then, C_{link} is connected to the SSCB through S_1 for the subsequent short-circuit fault test. Therefore, when S_2 is closed, the dynamic response of the proposed SSCB is tested for a short-circuit fault, while the fault resistance R_{fault} is set to 3 Ω.

Figure 12 shows the SSCB experimental waveforms obtained during the short-circuit fault isolation process.

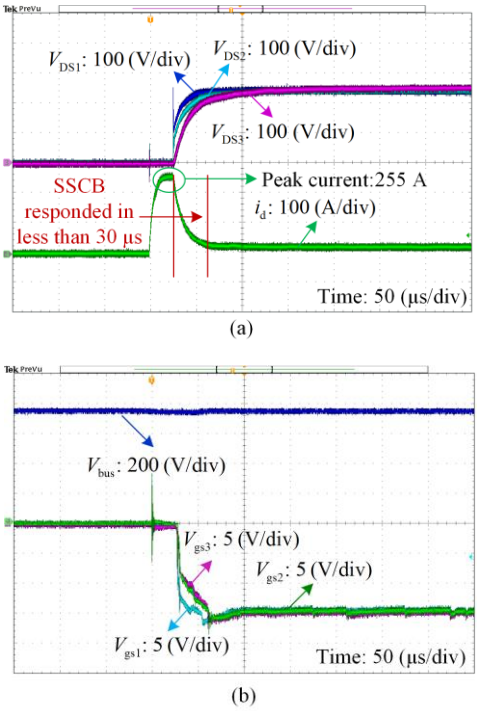


Fig. 12. Experimental waveforms of the SSCB during a short-circuit fault isolation process. (a) Drain-source voltages V_{DS1}, V_{DS2} and V_{DS3} and short-circuit current i_d. (b) Gate-source voltages V_{gs1}, V_{gs2} and V_{gs3} and DC-link voltage V_{bus}.

As shown in Fig. 12(a), when a short-circuit fault occurs, the current i_d flowing through the cascaded SiC JFETs (J_1, J_2, and J_3) of the SSCB rapidly increases from zero to 255 A (approximately 4 times the SiC JFET nominal current). At this point, the SSCB gate driver responds rapidly to the fault. The microprocessor sends a bias voltage of −15 V to the gate of J_1. The gate-source voltages V_{gs1}, V_{gs2}, and V_{gs3} of J_1, J_2, and J_3 reduce from zero to −15 V, respectively, as shown in Fig. 12(b). Thus, the SiC JFETs are turned off individually, and the action response time of the SSCB is approximately 30 μs. During the SSCB turn-off process, the drain-source voltages V_{DS1}, V_{DS2}, and V_{DS3} of the cascaded SiC JFETs successively increase from zero to approximately 250 V, as shown in Fig. 12(a), with no overvoltage observed. When the SSCB is completely turned off, V_{DS1}, V_{DS2}, and V_{DS3} are maintained at approximately 250 V. Thus a balanced distribution of the drain-source voltages in the SiC JFET series circuit is realized.

B. Overcurrent Experimental Results

To evaluate the SSCB performance for an overcurrent event, the voltage V_{bus} is also 750 V while the resistance R_{fault} is set to 6 Ω. Therefore, when S_2 is closed, an overcurrent is simulated. From the maximum thermal capacity of the SiC JFET for different overcurrent values, the PWM current-limiting delay interval T_d is set to 1.8 ms when the overcurrent is twice that of the SiC JFET nominal current.

Figure 13 shows the SSCB experimental waveforms for the overcurrent event. It shows that when S_2 is turned on, i_d quickly increases from zero to 130 A (approximately twice the SiC JFET nominal current). Based on the overcurrent protection principle, to effectively determine whether i_d is a persistent overcurrent or an inrush current generated by capacitive load startup, the microprocessor sends a PWM control signal with a delay interval of 1.8 ms to the gate of J_1. At the end of the PWM mode, i_d is still larger than the SiC JFET nominal current (63 A), while the load voltage V_o is approximately 660 V, which satisfies the inequality $|V_{bus} - V_o|/V_{bus} > 10\%$. Therefore, the SSCB infers that i_d is an overcurrent, and the microprocessor sends a bias voltage signal (−15 V) to the gate of J_1 to turn off the SSCB. Thus, the overcurrent protection of the SSCB is realized. Figure 13 shows that when the SSCB is turned off, the overvoltage suppression effect of the drain-source voltages V_{DS1}, V_{DS2}, and V_{DS3} of J_1, J_2, and J_3 are optimal. Simultaneously, the designed SSCB achieves balanced dynamic and static distributions of the drain-source voltages of the SiC JFETs.

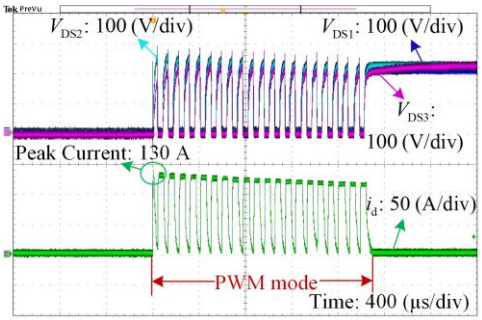


Fig. 13. Experimental waveforms of the SSCB for an overcurrent event.

C. Inrush Current Experimental Results

For the test circuit shown in Fig. 11, if C_{load} (100 μF) is connected in parallel at both ends of the fault resistance R_{fault} (20 Ω) with S_3, the inrush current caused by the capacitive load startup can be simulated by controlling S_3. In this test, V_{bus} is also set to 750 V.

Figure 14 gives the test waveforms of the SSCB for the capacitive load event. After the capacitive load starts up, the inrush current i_d, owing to the influence of the capacitor C_{load}, increases rapidly from 0 to approximately 120 A. Similarly, to determine whether i_d is caused by an overcurrent fault or capacitive load operation, the SSCB

enters into the PWM mode with a delay of 1.8 ms. During the PWM mode, the charging process of C_{load} is gradually completed. When the PWM mode ends, i_{d} decreases to approximately 37 A, which is within the operating range of the SiC JFET nominal current. At this point, voltage V_{o} also satisfies the inequality $|V_{\text{bus}}-V_{\text{o}}|/V_{\text{bus}} \leqslant 10\%$. The SSCB infers that i_{d} is the inrush current generated during normal capacitive load startup. Therefore, a 0 V drive signal is applied to the gate of the SiC JFETs to enable the SSCB to operate normally.

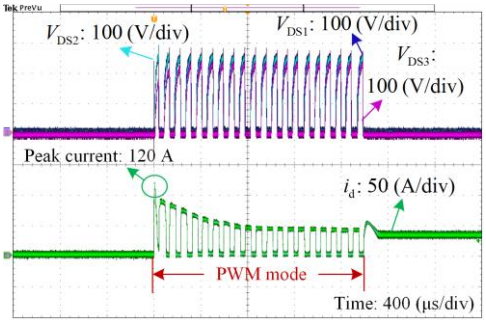


Fig. 14. Experimental results of the SSCB during an inrush current condition.

D. Fault Recovery Experimental Results

After a fault in the DC system is removed, the SSCB is turned on and the DC distribution system resumes normal operation. Figure 15 shows the experimental waveforms of the SSCB during the turn-on process.

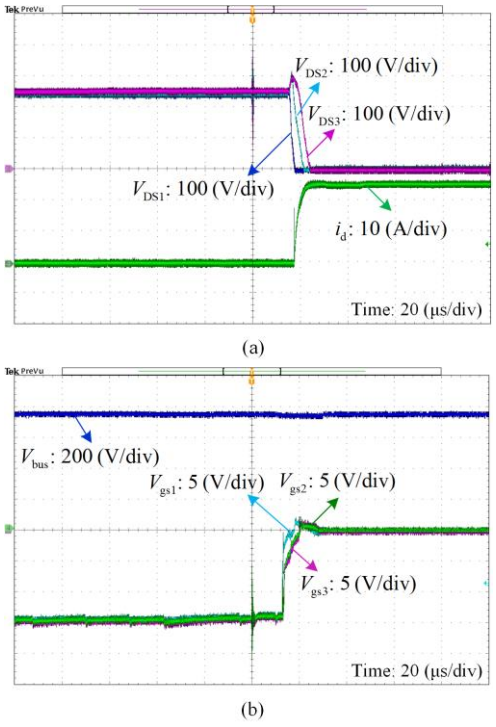


Fig. 15. Experimental waveforms obtained when the SSCB is restored to normal operation. (a) Drain-source voltages V_{DS1}, V_{DS2} and V_{DS3} and load current i_{d}. (b) Gate-source voltages V_{gs1}, V_{gs2} and V_{gs3} and DC-link voltage V_{bus}.

The voltage V_{bus} and load resistance R_{fault} are set to 750 V and 30 Ω, respectively. As shown in Fig. 15(b), when the DC fault is removed, the SSCB drive circuit sends a turn-on signal (0 V) to the gate of J_1. At this time, the gate-source voltage V_{gs1} of J_1 increases from −15 V to zero, i.e., J_1 is switched from the off state to the on state. Therefore, the drain-source voltage V_{DS1} of J_1 gradually decreases from 250 V to zero, as shown in Fig. 15(a). During the turn-on process of J_1, J_2 and J_3 are turned on individually, and the corresponding drain-source voltages V_{DS2} and V_{DS3} are gradually reduced from 250 V to zero. The load current i_{d} also increases from zero to approximately 25 A. The drain-source voltages V_{DS1}, V_{DS2}, and V_{DS3} do not exhibit significant overshoots during the SSCB turn-on process. The time required for the SSCB to be fully turned on is under 20 μs.

VI. CONCLUSION

To fulfill the requirements of SiC-based SSCB applications at medium-voltage level, the series operation of solid-state SiC devices is an economical and feasible way to improve their applicability. In this study, a 1.5 kV, 63 A medium-voltage SSCB based on cascaded normally-on SiC JFETs is presented. The SSCB consists of three main components: a signal sampling circuit, a microprocessor control unit, and a main static switch composed of three SiC JFETs in series. A programmable gate driver design facilitates good dynamic and static voltage sharing of the SiC JFETs during series operation, thus effectively suppressing the overvoltage during the turn-on and turn-off processes of the SSCB. The key parameters and selection conditions of the SSCB gate driver are analyzed, thus providing a useful reference for the practical design of an SSCB for medium-voltage DC distribution protection. Additionally, an improved PWM current-limiting protection approach is presented to realize fast short-circuit and overcurrent protection, and to avoid maloperation of the SSCB owing to the transient inrush current. The proposed method is validated based on interruption tests of an SSCB prototype. The test results reveal that the designed SSCB achieves reliable protection against different fault conditions and is effective for the series operation of SiC devices. This has important practical significance in ensuring the safe and stable operation of medium-voltage DC distribution networks.

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AUTHORS' CONTRIBUTIONS

Dong He：proposed the innovative points and drafted the original manuscript. Haohui Zhou: analyzed the data and contributed to writing the original draft of the manuscript. Zheng Lan: contributed to writing the original draft of the manuscript. Wei Wang: investigated the voltage equalization method and research background of medium-voltage SSCBs. Jinhui Zeng: conducted experiments and verified the accuracy of the results. Xueping Yu: checked and revised English expression. Z. John Shen: provided theoretical guidance. All authors read and approved the final manuscript.

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AVAILABILITY OF DATA AND MATERIALS

Not applicable.

DECLARATIONS

Competing interests: The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this article.

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