# Microgrid Fault Detection Method Coordinated with a Sequence Component Current-Based Fault Control Strategy

Zihao Wang and Longhua Mu

***Abstract*—The fault characteristics of microgrids are affected by the penetration of inverter-interfaced distributed generators (IIDGs). It makes conventional protection schemes no longer applicable. With different grid codes in different countries, IIDGs need to adopt different positive-sequence low-voltage ride-through (LVRT) control strategies during LVRT. Therefore, conventional protection schemes have to be modified according to the specific microgrid structure and the IIDGs' LVRT strategy. In order to adapt to different grid codes, a sequence component current-based fault control strategy and a coordinated microgrid fault detection method are proposed in this paper. The fault control strategy of IIDGs comprehensively considers the coordination between voltage support and fault characteristics generation, where the sequence currents are controlled separately. The positive-sequence current control strategy aims at supporting the microgrid voltage, whereas the negative-sequence current control strategy aims at generating or enhancing specific fault characteristics. Based on the proposed fault control strategy, the grid-feeding IIDGs can be equivalent to current sources and generate or enhance the negative-sequence fault characteristics in the equivalent additional networks of negative-sequence components. The fault feeder can then be accurately located by analyzing the phase relationship between the negative-sequence fault components of voltage and current phasors. A coordinated microgrid fault detection method based on the fault control strategy of IIDGs is proposed. The proposed fault control method makes the fault component protection principle applicable to all types of faults under any operational modes of microgrids. Finally, the correctness and effectiveness of the proposed coordinated fault control and protection strategy are verified in PSCAD/EMTDC.**

***Index Terms*—Microgrid protection, coordination of control and protection, fault characteristics, fault component.**

## I. Introduction

Inverter-interfaced distributed generators (IIDGs) formed by distributed power supplies are connected to a microgrid through power electronic devices [1], [2]. The microgrid is an important part of a power system in which IIDGs can help to maintain bus voltage and frequency stability, supply energy and generate specific fault characteristics. However, the plug-and-play of IIDGs changes the topology of a microgrid and raises a difficulty in fault detection and protection [3], [4].

In a traditional power system powered by only one synchronous generator (SG), the current direction is unidirectional from the SG to the load side. On the other hand, with the connection of IIDGs the current direction is now bidirectional so that the conventional unidirectional current-based protection schemes are no longer suitable [5]. A protection scheme using solid-state unidirectional fault current limiter to limit the downstream fault current is proposed in [6], and both protection and power quality issues are considered. However, this method requires additional hardware in the microgrid, which is an uneconomic solution. Reference [7] proposes a multiterminal hybrid differential protection scheme based on a wireless communication network. Thus the impact of IIDGs can be reduced, but the overall hardware cost will increase. To deal with the problem of low fault current level in a microgrid with IIDGs, an adaptive over-current protection scheme is proposed in [8]. Based on traditional over-current protection, this method adaptively modifies the threshold of current relays to accommodate the connection of IIDGs. Similarly, some improved current-based protection schemes are presented in [9]–[12], but they cannot protect islanded microgrids effectively owing to the low short-circuit current contribution of IIDGs.

With a fault inception in a microgrid, IIDGs should adopt the low voltage ride-through (LVRT) control strategy to stay connected and support the system. The LVRT criterion specifies the positive-sequence current during the fault, and the LVRT control strategies are different for different national grid codes. In LVRT mode, [13] analyzes the fault characteristics and pro-

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poses corresponding fault detection methods and protection schemes. Combined with the LVRT control strategy, specific fault characteristics can be generated by fault control strategies of IIDGs in specific scenarios. In [14], [15], different off-nominal frequency signals are generated by IIDGs to form superimposed networks based on these specific frequencies, and conventional fault detection methods can then be applied in these superimposed networks. However, some types of IIDGs and loads may show low resistance characteristics at certain frequencies and absorb most of these signals. Therefore these methods may not be reliable for complex microgrids. An auxiliary voltage controller is proposed in [16] to enhance the fault characteristics for a transient monitoring function-based fault detection method. Methods of generating or mimicking the fault characteristics of an SG are also presented in [17], [18]. During faults, IIDGs will imitate the output current characteristic of an SG, so that the distance protection and fault phase selection methods can still be applicable. Therefore the fault control strategy and protection coordination design that can generate or enhance the specific fault characteristics is the state-of-the-art technology to deal with the challenges of microgrid protection.

Different control strategies of IIDGs will affect the electrical characteristics of a microgrid and the fault characteristics. Owing to the controllability of IIDGs, fault characteristics can be generated in multiple coordinate systems or networks. A third harmonic voltage injection method is proposed in [19], in which the specific frequency voltage component injected by IIDGs forms a specific frequency superimposed network. Then, a coordinating harmonic time-current-voltage directional relay is designed to detect specific frequency fault characteristics. For a three-phase system, the three-phase electrical signals can be decomposed into positive-, negative-, and zero-sequence components. These decoupled sequence components can be controlled by IIDGs independently and used as fault characteristics [20]. Reference [21] reveals the impact of positive- and negative-sequence output power of an IIDG on microgrid voltage, and the fault component principle is adopted to develop the fault models and fault calculation method of the microgrid. However, this work mainly concentrates on the positive-sequence fault component, while the negative-sequence fault models and the corresponding fault detection methods still need further study.

Asymmetrical faults are common in a microgrid, and thus the negative-sequence components can be used as fault characteristics in these cases. However, when an asymmetrical high-impedance fault occurs, the negative-sequence fault characteristics in the microgrid are not obvious. In addition, there is no negative-sequence component when a symmetrical fault occurs. To address these problems, a sequence current-based fault control strategy and a coordinated fault detection method are proposed in this paper. A typical master-slave controlled microgrid is analyzed, one which contains grid-forming and grid-feeding IIDGs. The symmetrical component method is used to analyze the fault characteristics in different fault conditions. The fault component principle is applied to fault modeling, and its limitation with penetration of IIDGs is introduced. Then a sequence component current-based fault control strategy is proposed. With a fault inception, the phases of negative-sequence fault currents are determined and the amplitudes of negative-sequence fault currents are strengthened by grid-feeding IIDGs. The specific fault characteristics exist in both symmetrical and asymmetrical fault conditions so that the conventional fault component protection principle is still valid. Based on these negative-sequence fault characteristics, a new fault detection method is presented. By monitoring the negative-sequence fault components on buses, the fault feeder can be accurately located. Finally, the effectiveness of the proposed negative-sequence current-based fault control strategy and fault detection method is verified by PSCAD/EMTDC.

This remainder of the paper is organized as follows. Section II presents the relationship between fault types and symmetrical components, and indicates the applicability and limitation of the fault component principle. A sequence component current-based fault control strategy is proposed in Section III, and Section IV analyzes the fault components and proposes a new fault detection method. The effectiveness and correctness of the proposed control strategy and detection method are verified by PSCAD/EMTDC in Section V. Section VI concludes the paper.

## II. Applicability Analysis of Fault Component Principle

### A. Fault Types and Symmetrical Component Method

Assuming that under normal operation of a three-phase SG system without IIDG, the magnitudes of the three-phase voltages are equal while their phase differences are 120°. When an asymmetrical fault occurs, the phase voltages become asymmetrical and the amplitudes are no longer equal. The imbalance degree is dependent on the fault type.

Using the symmetrical component method, a three-phase sinusoidal signal can be decomposed into a set of positive-, negative-, and zero-sequence signals. In medium- or low-voltage microgrids, the ungrounded mode is adopted so that there is no zero-sequence component.

In normal operational conditions, the phase voltages are symmetrical, and thus only positive-sequence components exist. When line-to-ground and line-to-line (to-ground) faults occur, the negative-sequence compo-

nents appear. Taking a phase-A-to-ground (AG) fault and a phase-B-to-phase-C (to-ground) (BC or BCG) fault as examples, the composite phasor diagrams are shown in Fig. 1.

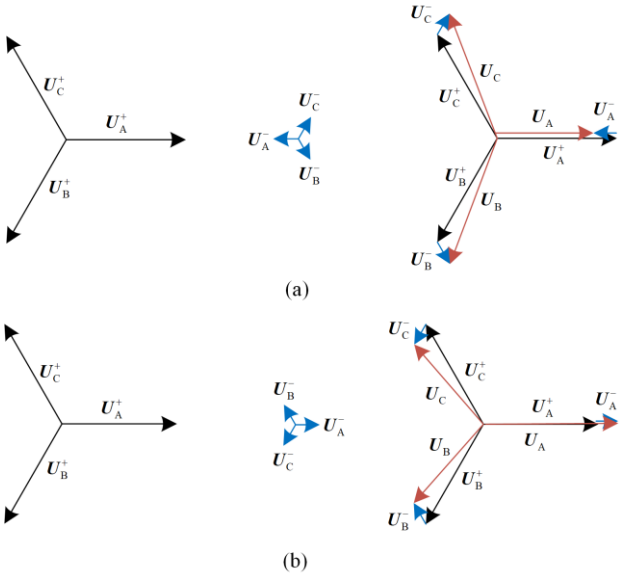


Fig.1. The composite voltage phasor diagrams of faults. (a) Phase A-to-ground fault. (b) Phase B-to-phase C (to-ground) fault.

Figure 1(a) shows the composite voltage phasor diagram when there is an AG fault. In this case, the voltage amplitude of phase A is the smallest and the voltage amplitudes of the other two phases are equal. The phase difference between the positive- and negative-sequence components is 180°. Figure 1(b) shows the composite voltage phasor diagram when there is a BC(G) fault, where the voltage amplitude of phase A is the largest and the voltage amplitudes of other two phases are equal. The phase difference between the positive- and negative-sequence voltage components is 0°.

When a fault occurs, the phase angle of the positive-sequence voltage will decrease. On the other hand, the phase angles of the negative-sequence voltage components are quite different and dependent on the fault type. The analysis method in Fig. 1 can be applied to other fault types. The relationships between the positive- and negative-sequence voltages and fault types are shown in Table I.

However, with penetration of IIDGs, these phase relationships are affected such that the traditional protection method for an SG system is no longer valid.

TABLE I
PHASE DIFFERENCES BETWEEN POSITIVE-AND NEGATIVE-SEQUENCE VOLTAGE COMPONENTS

| Fault type | AG | BC(G) | BG | AC(G) | CG | AB(G) |
|---|---|---|---|---|---|---|
| Phase difference(°) | 180 | 0 | −60 | 120 | 60 | −120 |

### *B. The Fault Component Principle*

According to the superposition principle, any current or voltage signal can be considered as the sum of two components: normal-running and fault components. The fault component can be calculated using superimposed networks [22]. Assuming that $i_n(t)$ and $v_n(t)$ are the current and voltage of the normal-running system, while $i_f(t)$ and $v_f(t)$ are the current and voltage of the faulted system, the fault components $\Delta i_f(t)$ and $\Delta v_f(t)$ can be expressed as:

$$\begin{cases} \Delta i_f(t) = i_f(t) - i_n(t) \\ \Delta v_f(t) = v_f(t) - v_n(t) \end{cases} \tag{1}$$

As (1) indicates, the fault component of current or voltage can be calculated by subtracting the normal-running (pre-fault) current or voltage from the post-fault current or voltage. Thus, the fault components do not exist in normal conditions but will appear if a fault occurs in the microgrid.

The fault component principle can be applied to different sequence components, such as positive- and negative-sequence components. Similarly, since the positive- and negative-sequence components are decoupled, they can be controlled and analyzed separately.

### *C. Applicability and Limitation of the Fault Component Principle*

The fault component principle is a powerful tool to analyze faults in microgrids. Combined with the symmetrical component method, the fault component principle can be adopted in positive-, negative- and zero-sequence component networks.

A simplified structure of an ungrounded microgrid is shown in Fig. 2(a). The utility grid, or a grid-forming IIDG, or a diesel generator, maintains the voltage and frequency stability of the microgrid. A grid-feeding IIDG like a Type-4 wind turbine or photovoltaic cell is connected to provide power. In Fig. 2, $Z_{Feeder}$ is the feeder impedance. Since the positive- and negative-sequence impedances are almost equal, they are both represented by $Z_{Feeder1}$ and $Z_{Feeder2}$. When a fault occurs on the feeder, the equivalent additional network of the positive-sequence fault component can be established as shown in Fig. 2(b). $Z_{Grid}$ is the impedance of the utility grid or the grid-forming IIDG, $\Delta \boldsymbol{u}_f^+$ is the additional positive-sequence voltage source at the fault point, and $R_f$ is the fault resistance. According to the German grid code, the grid-feeding IIDG should output positive-sequence power to the microgrid during the fault. Thus, it can be equivalent to an additional positive-sequence current source $\boldsymbol{i}_{IIDG.f}$ controlled by the positive-sequence voltage at point of coupling (PC) [13]. Since the positive-sequence fault components exist under both symmetric and asymmetric faults, the model in Fig. 2(b) is always valid. However, because of the

plug-and-play of IIDGs, the fault characteristics may be affected.

When an asymmetrical fault occurs on the feeder, the equivalent additional network of negative-sequence fault component is shown in Fig. 2(c). The asymmetric fault leads to the emergence of an additional negative-sequence voltage source $\Delta \boldsymbol{u}_{\mathrm{f}}^{-}$. Since the IIDG does not output negative-sequence current, it can be equivalent to impedance $Z_{\mathrm{IIDG}}$. Thus, the connection of IIDG changes the total impedance of the system, and affects the fault characteristics.

When a symmetrical fault occurs on the feeder, Fig. 2(c) will be transformed into Fig. 2(d). Since the symmetrical fault will not lead to the emergence of a negative-sequence voltage source, Fig. 2(d) is a passive network. Therefore, there will be no negative-sequence fault component in this network.

Owing to IIDGs' varied control strategies, connecting positions and grid codes, the sequence component networks in Fig. 2 will be affected by the connection of IIDGs. The fault characteristics of a microgrid will also change with the penetration of IIDGs. Hence, the applicability of the protection schemes based on the fault component principle is limited.

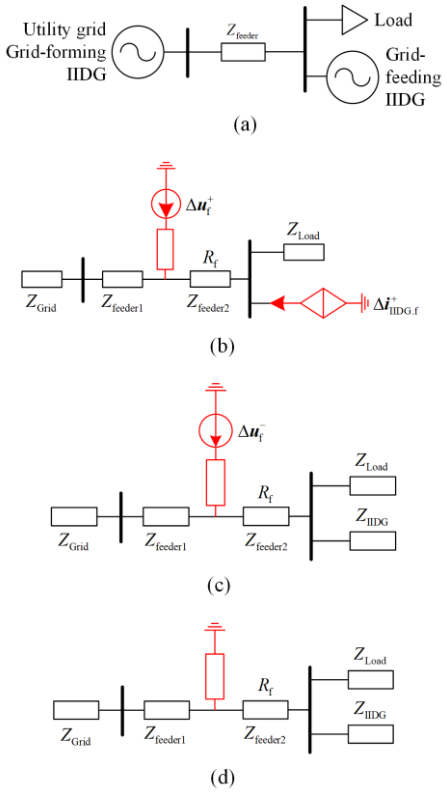


Fig.2. Simplified microgrid and equivalent additional sequence component networks. (a) Simplified structure of microgrid. (b) Positive-sequence network. (c) Negative-sequence network under asymmetrical fault. (d) Negative-sequence network under symmetrical fault.

## III. A Sequence Component Current-Based Fault Control Strategy

From the analysis represented by Fig. 2, it can be concluded that sequence component networks can be controlled independently by IIDGs' sequence component control strategies. When a microgrid is in a fault condition, IIDGs should adopt the LVRT control strategy to remain connected. In a medium-voltage system, IIDGs are required to output reactive power to support the grid voltage. This will affect the sequence component networks and fault characteristics of the microgrid. Therefore, in the LVRT mode, the fault control strategy of IIDGs should also consider coordination between grid voltage support and fault characteristics enhancement of microgrid protection.

In this paper, a sequence component current-based fault control strategy is proposed as shown in Fig. 3. The fault control strategy is coordinated with grid voltage support in the positive-sequence component network and fault characteristic enhancement in the negative-sequence component network.

### *A. The Positive-Sequence Current Control Strategy*

For the grid-feeding IIDGs, the control object is to output a constant current to provide a constant positive-sequence power. In the synchronous rotating reference orthogonal coordinate, the average value of positive-sequence active power $P_{\mathrm{out}}^{+}$ and reactive power $Q_{\mathrm{out}}^{+}$ of an IIDG can be expressed as:

$$\begin{cases} P_{\mathrm{out}}^{+} = \dfrac{3}{2} U_d^{+} I_{\mathrm{ref}.d}^{+} \\ Q_{\mathrm{out}}^{+} = -\dfrac{3}{2} U_d^{+} I_{\mathrm{ref}.q}^{+} \end{cases} \tag{2}$$

where $U_d^{+}$ represents the $d$-axis positive-sequence voltage amplitude at PC; $I_{\mathrm{ref}.d}^{+}$ and $I_{\mathrm{ref}.q}^{+}$ represent the $d$-axis and $q$-axis components of positive-sequence current reference signal $I_{\mathrm{ref}}$ respectively.

When a fault occurs in the microgrid, the grid-feeding IIDGs should output positive-sequence reactive current $I_{\mathrm{LVRT}.q}^{+}$ to support the grid voltage, described as:

$$I_{\mathrm{LVRT}.q}^{+} = \begin{cases} 0, & 0.9U_{\mathrm{rate}} < U_{\mathrm{f}.d}^{+} \leqslant U_{\mathrm{rate}} \\ k_{\mathrm{p}} k_{\mathrm{c}} I_{\max} \left(1 - \dfrac{U_{\mathrm{f}.d}^{+}}{U_{\mathrm{rate}}}\right), & U_{\min} < U_{\mathrm{f}.d}^{+} \leqslant 0.9U_{\mathrm{rate}} \\ I_{\max} - I_{\mathrm{Fault}}^{-}, & 0 < U_{\mathrm{f}.d}^{+} \leqslant U_{\min} \end{cases} \tag{3}$$

where $U_{\mathrm{f}.d}^{+}$ is the $d$-axis positive-sequence fault voltage at PC; $U_{\min}$ is the voltage when $I_{\mathrm{LVRT}.q}^{+}$ reaches the maximum value; $U_{\mathrm{rate}}$ is the rated voltage; $k_{\mathrm{p}}$ is the support rate of the positive-sequence current determined by the national grid code; $k_{\mathrm{c}}$ is the vector compression

rate determined in (6); $I_{\max}$ is the maximum output current of IIDG; and $I_{\text{Fault}}^{-}$ is the negative-sequence output current during the fault.

The proposed positive-sequence fault control scheme is shown in Fig. 3(a), where $\boldsymbol{i}$ and $\boldsymbol{u}_{\text{c}}$ represent the output current and capacitor voltage of the IIDG, respectively. In Fig. 3, the superscripts "+" and "–" represent the positive- and negative- sequence components of the electrical quantities. From (3), it is concluded that when the fault severity is light, i.e., $U_{\text{f}.d}^{+} > 0.9U_{\text{rate}}$, the grid-feeding IIDGs will not output additional positive-sequence reactive current. Thus, different fault voltage levels will lead to different positive-sequence fault characteristics. This will also lead to the failure of the positive-sequence fault component protection principle.

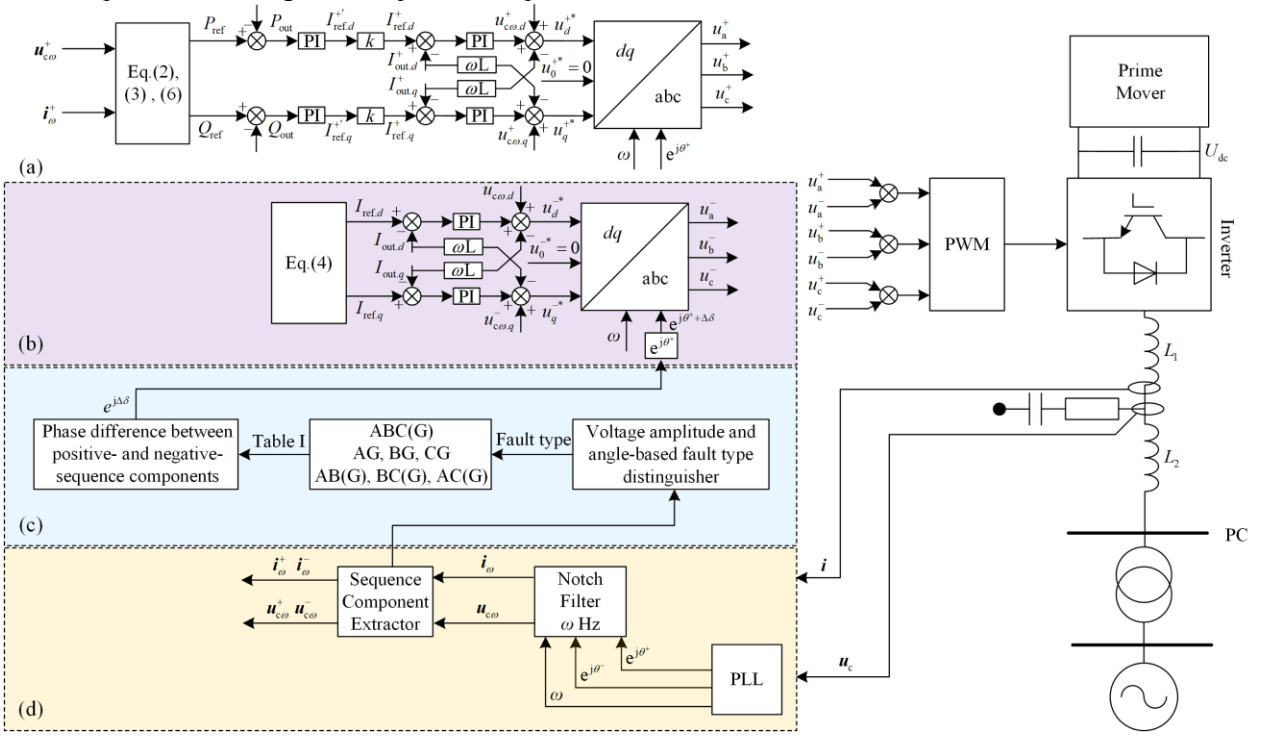


Fig. 3. The control structure of sequence component current-based fault control strategy. (a) Positive-sequence Control. (b) Negative-sequence Control. (c) Fault type distinguishing. (d) Angle and amplitude extracted.

### *B. Negative-Sequence Current-Based Fault Control Strategy*

To solve the problem of different fault characteristics at different fault voltage levels, the proposed negative-sequence current-based fault control strategy should generate the specific negative-sequence fault characteristics during grid faults. From the analysis represented in Fig. 2(c), a negative-sequence voltage source will appear during an asymmetrical fault. Thus, in order to make the proposed negative-sequence current-based fault control strategy valid for both symmetrical and asymmetrical faults, the phase and amplitude of IIDG output current should be considered comprehensively.

In contrast to the additional positive-sequence reactive current output which does not exist when the fault severity is light, the negative-sequence fault current output should always be retained during a grid fault regardless of the fault severity. The amplitude of the negative-sequence fault current is:

$$I_{\text{Fault}}^{-} = \begin{cases} I_{\text{Neg}}, & U_{\text{f}.d}^{+} \leqslant 0.9U_{\text{rate}} \\ 0.5I_{\text{Neg}} + 5(1 - \dfrac{U_{\text{f}.d}^{+}}{U_{\text{rate}}})I_{\text{Neg}}, & 0.9U_{\text{rate}} < U_{\text{f}.d}^{+} \leqslant U_{\text{rate}} \\ 0, & U_{\text{f}.d}^{+} = U_{\text{rate}} \end{cases} \tag{4}$$

where $I_{\text{Neg}}$ is the amplitude of the maximum negative-sequence output current.

Because the positive-sequence fault voltage exists in all types of faults and can directly reflect the fault severity, the negative-sequence fault current is set to be controlled by $U_{\text{f}.d}^{+}$. Figure 3(b) illustrates the proposed negative-sequence current-based fault control scheme.

Based on the proposed negative-sequence current-based fault control strategy, the IIDGs will output negative-sequence current when a voltage sag occurs. The negative-sequence output current reaches its maximum value when the voltage sag is more than 10%. At that time, the sequence component networks in Figs. 2 (c) and (d) will be transformed into Figs. 4 (a) and (b),

respectively. When a symmetrical or asymmetrical fault occurs, the IIDGs will always output the negative-sequence fault current. In other words, the negative-sequence fault characteristics will always exist. In Fig. 4(a), the negative-sequence fault characteristics will be enhanced by IIDGs, while Fig. 4(b) shows a single power supply structure. For a multiple IIDGs-based microgrid, the negative-sequence fault characteristics will be generated and enhanced during symmetrical faults. Therefore, the proposed negative-sequence current-based fault control strategy will extend the applicability of the fault component protection principle.

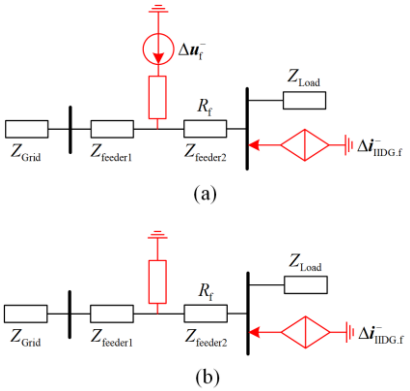


Fig. 4. Simplified microgrid and equivalent additional sequence component networks with sequence current-based fault control strategy. (a) Negative-sequence network under an asymmetrical fault. (b) Negative-sequence network under a symmetrical fault.

### *C. Composite Sequence Component Fault Control Strategye*

The sequence component current-based fault control strategy needs to comprehensively consider the current limitation, and the positive- and negative-sequence current control. The control block diagram of the composite sequence component current control strategy has been shown in Fig. 3.

In Fig. 3(d), the phase locked loop (PLL) block calculates the angular frequency $\omega$, positive-sequence PC voltage angle $\theta^+$ and negative-sequence PC voltage angle $\theta^-$. A notch filter is combined with the PLL block to extract the IIDG output current $\boldsymbol{i}$, the capacitor voltage $\boldsymbol{u}_c$, and the PC voltage $\boldsymbol{u}$ at the angular frequency $\omega$. In particular, $\omega$ is set to 314 rad/s in this paper for the 50 Hz system. A sequence component extractor is adopted to extract the positive- and negative-sequence components of voltages and currents.

The fault type distinguishing block diagram is shown in Fig. 3(c). When a fault occurs, the most important thing is to distinguish the fault type and then determine the phase difference between the positive- and negative-sequence voltage components. A fault type detection method using PC voltage proposed in [23] is adopted in this paper. By referring to Table I, the phase difference can be determined. As a result, the negative-sequence current controller, as shown in Fig. 3(b), will regulate the phase of the negative-sequence output current of IIDGs close to that of the additional negative-sequence voltage source. Therefore, as shown in Figs. 4 (a) and (b), the negative-sequence fault characteristics will be generated during symmetrical faults and enhanced for asymmetrical faults.

To simplify the analysis, it is assumed that the output electrical quantities of IIDGs can track their reference values. For the negative-sequence control block, the current amplitude is determined by (4), and the phase difference $\Delta\delta$ is determined in the fault type distinguishing block. Thus, the instantaneous value of the negative-sequence current in abc coordinates, namely $i_a^-$, $i_b^-$ and $i_c^-$, can be expressed as:

$$\begin{cases} i_a^- = I_{Fault}^- \cos(\omega t + \theta^+ + \Delta\delta) \\ i_b^- = I_{Fault}^- \cos\left(\omega t + \theta^+ + \Delta\delta + \dfrac{2\pi}{3}\right) \\ i_c^- = I_{Fault}^- \cos\left(\omega t + \theta^+ + \Delta\delta - \dfrac{2\pi}{3}\right) \end{cases} \tag{5}$$

The positive-sequence current control strategy should pay attention to the amplitude of the negative-sequence output current and the current limit issue. As the voltage sag increases, the output current reaches its limit, and thus the reference value of the positive-sequence current should be compressed accordingly. The vector compression rate $k_c$ can be expressed as:

$$k_c = \begin{cases} 1, & \left(I_{Fault}^- + \sqrt{(I_{ref.d}^{+'})^2 + (I_{ref.q}^{+'})^2} \leqslant I_{max}\right) \\ \dfrac{I_{max} - I_{Fault}^-}{\sqrt{(I_{ref.d}^{+'})^2 + (I_{ref.q}^{+'})^2}}, & \left(I_{Fault}^- + \sqrt{(I_{ref.d}^{+'})^2 + (I_{ref.q}^{+'})^2} > I_{max}\right) \end{cases} \tag{6}$$

where $I_{ref.d}^{+'}$ and $I_{ref.q}^{+'}$ are the uncompressed reference values of the $d$- and $q$-axis currents, respectively.

Thus, the instantaneous values of the positive-sequence output current in abc coordinates can be expressed as:

$$\begin{cases} i_a^+ = I_{Fault}^+ \cos(\omega t + \theta^+) \\ i_b^+ = I_{Fault}^+ \cos\left(\omega t + \theta^+ - \dfrac{2\pi}{3}\right) \\ i_c^+ = I_{Fault}^+ \cos\left(\omega t + \theta^+ + \dfrac{2\pi}{3}\right) \end{cases} \tag{7}$$

where $I_{Fault}^+$ is the amplitude of the positive-sequence fault current, expressed as:

$$I_{Fault}^+ = \sqrt{(I_{ref.d}^+)^2 + (I_{ref.q}^+)^2} \tag{8}$$

where $I_{ref.d}^+$ and $I_{ref.q}^+$ are the corresponding compressed reference values.

## IV. A New Microgrid Fault Detection Method Based on the Sequence Component Current-Based Fault Control Strategy

### *A. Application of the Sequence Component Current-Based Fault Control Strategy*

From the IEEE 1547 standard, a microgrid model is shown in Fig. 5, where LD1–3 are loads, DG1–4 are IIDGs, A1–A4, B1–B4, C1–C3 and D1–D3 are the circuit breakers (CBs) of the feeders. The microgrid is connected to the utility grid through a PCC switch.

Specifically, DG2–DG4 represent the grid-feeding IIDGs like photovoltaics or Type-4 wind turbines. These adopt the negative-sequence current-based fault control strategy and thus can be equivalent to negative-sequence current sources in the equivalent negative-sequence additional network. DG1 represents a grid-forming IIDG like a diesel generator, which can be used as the main power source in the islanded microgrid to provide stable voltage and frequency for the bus. In particular, the main power source can only output positive-sequence voltage and thus can be equivalent to an impedance in the equivalent negative-sequence additional network.

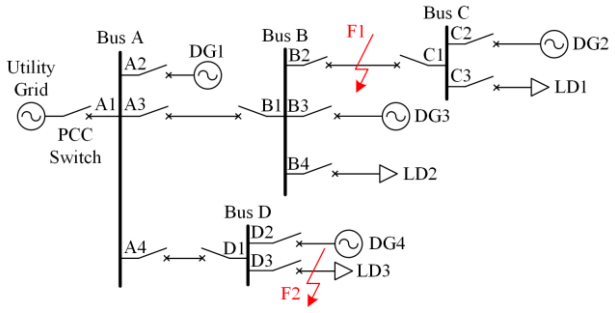


Fig. 5. Model of the microgrid.

Taking the F1 fault at feeder B2C1 in Fig. 5 as an example, the equivalent negative-sequence additional networks are shown in Fig. 6. Based on the proposed fault control strategy, the microgrid model can be decomposed into four equivalent additional networks. In the islanded mode in Figs. 6(a) and (b), the PCC switch is off. DG1 works as the main power source and can be equivalent to an impedance $Z_{\mathrm{DG1}}$. In the grid-connected mode in Figs. 6(c) and (d), the PCC switch is on, and $Z_{\mathrm{s}}$ represents the impedance of the utility grid. DG1 adopts the sequence component current-based fault control strategy and thus can be equivalent to an additional current source $\Delta\boldsymbol{i}_{\mathrm{DG1.f}}$. For the asymmetrical faults in Figs.6 (a) and (c), an additional negative-sequence voltage source $\Delta\boldsymbol{u}_{\mathrm{f}}^{-}$ is in series with a fault resistance $R_{\mathrm{f}}$ at the fault point. For the symmetrical faults in Figs. 6(b) and (d), there is only $R_{\mathrm{f}}$ at the fault point. In particular, the directions of the arrows in Fig. 6 represent the positive directions of currents.

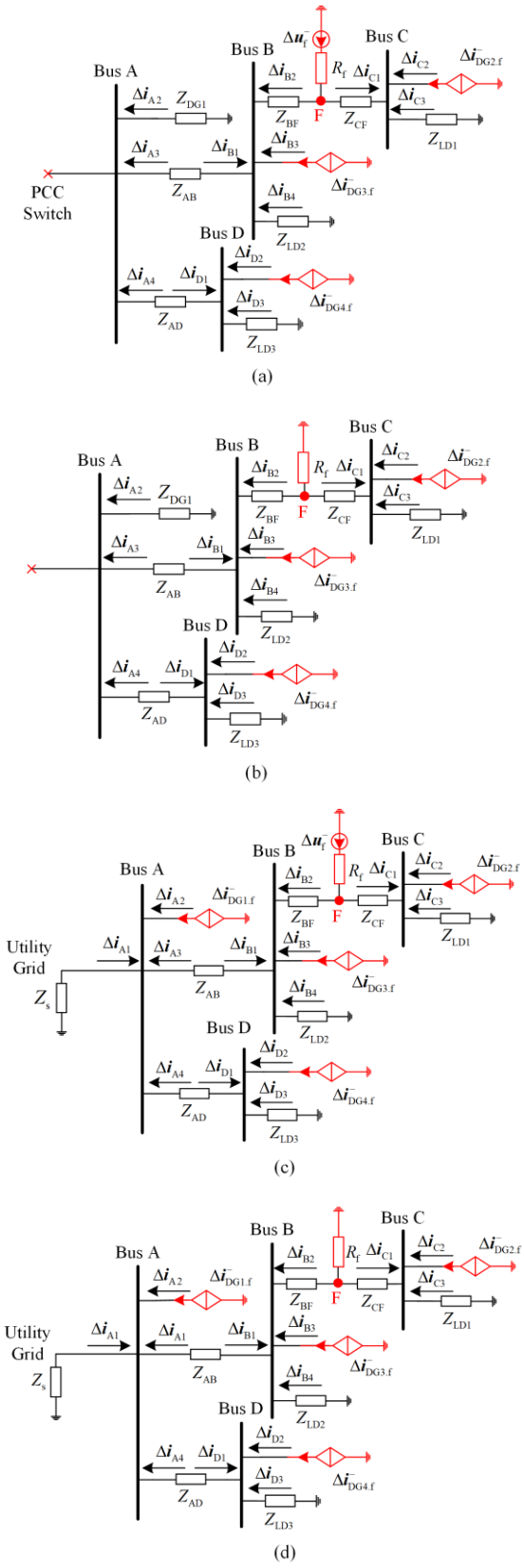


Fig. 6. Equivalent additional networks of negative-sequence fault components. (a) Asymmetrical fault in islanded mode. (b) Symmetrical fault in islanded mode. (c) Asymmetrical fault in grid-connected mode. (d) Symmetrical fault in grid-connected mode.

### B. Asymmetrical Fault at F1

Assuming that a BC(G) fault occurs at F1, the phase of the negative-sequence voltage is 0°. From Figs. 6 (a) and (c), the phasor diagrams of the negative-sequence fault components at feeder B2C1 are shown in Fig. 7, where Fig. 7(a) represents those of bus C and Fig. 7(b) represents those of bus B.

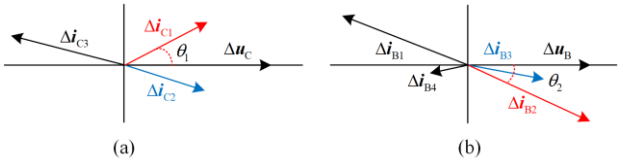


Fig. 7. Phasor diagrams of negative-sequence fault components under asymmetrical fault. (a) Bus C. (b) Bus B.

As shown in Fig. 7, at the fault feeder B2C1, $\Delta \boldsymbol{u}_{\mathrm{C}}$ and $\Delta \boldsymbol{u}_{\mathrm{B}}$ represent the respective negative-sequence voltage fault components at bus C and bus B. $\Delta \boldsymbol{i}_{\mathrm{C1}}$, $\Delta \boldsymbol{i}_{\mathrm{C2}}$ and $\Delta \boldsymbol{i}_{\mathrm{C3}}$ represent the respective negative-sequence current fault components at bus C, while $\Delta \boldsymbol{i}_{\mathrm{B1}}$, $\Delta \boldsymbol{i}_{\mathrm{B2}}$, $\Delta \boldsymbol{i}_{\mathrm{B3}}$ and $\Delta \boldsymbol{i}_{\mathrm{B4}}$ represent the respective negative-sequence current fault components at bus B. $\Delta \boldsymbol{i}_{\mathrm{C2}}$ and $\Delta \boldsymbol{i}_{\mathrm{B3}}$ are generated by IIDG2 and IIDG3, respectively, and their phase angles are close to that of the bus voltage. $\theta_1$ represents the phase difference between $\Delta \boldsymbol{u}_{\mathrm{C}}$ and $\Delta \boldsymbol{i}_{\mathrm{C1}}$, and $\theta_2$ represents the phase difference between $\Delta \boldsymbol{u}_{\mathrm{B}}$ and $\Delta \boldsymbol{i}_{\mathrm{B2}}$, both of which are in the range of 0° to 90° and are:

$$\begin{cases} \theta_1 = \left| \angle \Delta \boldsymbol{u}_{\mathrm{C}} - \angle \Delta \boldsymbol{i}_{\mathrm{C1}} \right| \\ \theta_2 = \left| \angle \Delta \boldsymbol{u}_{\mathrm{B}} - \angle \Delta \boldsymbol{i}_{\mathrm{B2}} \right| \\ 0° < \theta_1 < 90° \\ 0° < \theta_2 < 90° \end{cases} \tag{9}$$

For a non-fault feeder like A3B1, it is clear that (9) will not be satisfied, i.e., the phase difference of A3 is in the range of 0° to 90° whereas that of B1 is in the range of 90° to 180°.

### C. Symmetrical Fault at F1

According to Figs. 6 (b) and (d), for a symmetrical fault at F1, there is no additional voltage source at the fault point. Therefore, the negative-sequence fault components are only determined by the IIDGs. In symmetrical fault conditions, IIDGs will output the negative-sequence currents with a preset phase angle, which is 0° in this paper. The phasor diagrams of the negative-sequence fault components at feeder B2C1 when there is a symmetrical fault are shown in Fig. 8.

As shown in Figs. 8 (a) and (b), on the double-terminal feeders, the negative-sequence current fault components are mainly determined by the IIDGs. The direction of the negative-sequence current is from the IIDG to the fault point. Thus, the phase relationships can be described as:

$$\begin{cases} \theta_3 = \left| \angle \Delta \boldsymbol{u}_{\mathrm{C}} - \angle \Delta \boldsymbol{i}_{\mathrm{C1}} \right| \\ \theta_4 = \left| \angle \Delta \boldsymbol{u}_{\mathrm{B}} - \angle \Delta \boldsymbol{i}_{\mathrm{B2}} \right| \\ 90° < \theta_3 < 180° \\ 90° < \theta_4 < 180° \end{cases} \tag{10}$$

where $\theta_3$ represents the phase difference between $\Delta \boldsymbol{u}_{\mathrm{C}}$ and $\Delta \boldsymbol{i}_{\mathrm{C1}}$; and $\theta_4$ represents the phase difference between $\Delta \boldsymbol{u}_{\mathrm{B}}$ and $\Delta \boldsymbol{i}_{\mathrm{B2}}$, both of which are in the range of 0° to 90°.

For a non-fault feeder like A3B1, the phase difference of B1 is in the range of 0° to 90°, and that of A3 is in the range of 90° to 180°. Therefore, the phase differences of the two terminals are in different phase ranges.

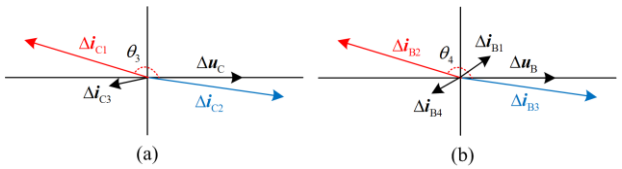


Fig. 8. Phasor diagrams of negative-sequence fault components under symmetrical fault. (a) Bus C. (b) Bus B.

### D. Asymmetrical Fault at F2

When an asymmetrical fault occurs at F2 in Fig. 5, the additional voltage source appears and the current phasor changes. The phasor diagram is shown in Fig. 9. $\Delta \boldsymbol{i}_{\mathrm{D1}}$, $\Delta \boldsymbol{i}_{\mathrm{D2}}$ and $\Delta \boldsymbol{i}_{\mathrm{D3}}$ represent the negative-sequence current fault components at bus D. $\theta_5$ represents the phase difference between $\Delta \boldsymbol{u}_{\mathrm{D}}$ and $\Delta \boldsymbol{i}_{\mathrm{D3}}$, which is in the range of 0° to 90°. Because of the voltage sag at the end of the feeder, the phase relationship can be described as:

$$\begin{cases} \theta_5 = \left| \angle \Delta \boldsymbol{u}_{\mathrm{D}} - \angle \Delta \boldsymbol{i}_{\mathrm{D3}} \right| \\ 0° < \theta_5 < 90° \end{cases} \tag{11}$$

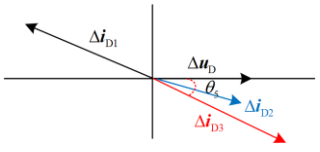


Fig. 9. Phasor diagram of negative-sequence fault components at bus D.

### E. Fault Starting Criterion

To deal with intermittency, it is necessary to design a fault starting criterion [13]. The IIDGs should determine whether to start fault characteristic generation, and the relays should determine whether to perform fault detection according to the starting criterion.

The amplitudes of the voltage fault components of the bus are selected as the starting criterion:

$$\left|\Delta \boldsymbol{u}^{+}\right|+\left|\Delta \boldsymbol{u}^{-}\right|+\left|\Delta \boldsymbol{u}^{0}\right|>U_{\text{set}} \tag{12}$$

where $\Delta \boldsymbol{u}^{+}$, $\Delta \boldsymbol{u}^{-}$, and $\Delta \boldsymbol{u}^{0}$ are the positive-, negative-, and zero-sequence voltage fault components of a bus respectively; $U_{\text{set}}$ is the starting threshold, and in this study, it is assumed to be $0.02\,U_{\text{rate}}$.

### *F. Negative-Sequence Fault Component Based Microgrid Fault Detection Method*

The proposed coordinating fault control and protection strategy consists of two parts: the fault control strategy of IIDGs and the protection strategy of the microgrid. The fault control strategy is responsible for generating fault characteristics, and the protection relays are responsible for detecting them. If (12) holds, the relays will perform fault detection based on the negative-sequence fault characteristics. By means of the sequence component current-based fault control strategy, specific negative-sequence fault characteristics are generated. Thus, the new microgrid fault detection method is summarized as follows:

1) For a faulted double-terminal feeder, according to (9) and (10), the phase differences between the negative-sequence voltage and current fault components at both terminals are in the same phase region, i.e., in the range of 0° to 90° or 90° to 180°. For a non-fault double-terminal feeder, the phase differences at its two terminals are in different phase ranges.

2) For an asymmetrical fault at the branch feeder, the phase difference between the negative-sequence voltage and current fault components is in the range of 0° to 90°. For a symmetrical fault, the phase difference is in the range of 90° to 180°.

## V. Simulation Results

To evaluate the correctness of the proposed method, the microgrid shown in Fig. 5 is simulated in PSCAD/EMTDC. The neutral point ungrounded mode is adopted in the microgrid. The voltage and frequency of the system are 10 kV (line-line, RMS) and 50 Hz, respectively. The grid-feeding IIDGs adopt the proposed sequence component current-based fault control strategy. The capacities of the grid-feeding IIDGs and grid-forming IIDG are 500 kVA and 2000 kVA, respectively. The capacities of the three-phase symmetrical loads LD1–3 are (1200+j30) kVA. The positive- and negative-sequence impedance of the feeders is (0.38+j0.45) Ω/km, and the zero-sequence impedance is (0.76+j1.32) Ω/km. The length of the feeders AB, BC and AD is 2 km, while the IIDGs and loads are connected to the bus through 0.1 km feeders. The maximum output fault current of the grid-feeding IIDGs and the grid-forming IIDG are 2 and 5 times their rated current respectively. $I_{\text{Neg}}$ is set to 10 A. The proposed fault control strategy mainly focuses on the negative-sequence fault characteristics. Thus, priority is given to the negative-sequence current output, and the positive-sequence current is vector compressed according to the output current limit. Therefore, the settings of the maximum output fault currents of the IIDGs will not affect the experimental results.

At 0.3 s, an asymmetrical fault occurs in the microgrid, and the current waveforms of IIDG2 are shown in Fig. 10. IIDGs should calculate the voltage sequence components to activate the negative-sequence fault characteristics output according to (12). This step takes one power frequency cycle. It can be seen from the current waveforms that IIDG2 adopts the proposed fault control strategy at 0.32 s, and quickly tracks the reference value and reaches steady state. The positive-sequence reactive current is generated according to the terminal positive-sequence voltage, while the negative-sequence current is generated according to the fault type. Then the relays will calculate the phase differences according to the negative-sequence fault characteristics in the microgrid. This also takes one cycle. Therefore, it only takes no more than 40 ms for fault detection.

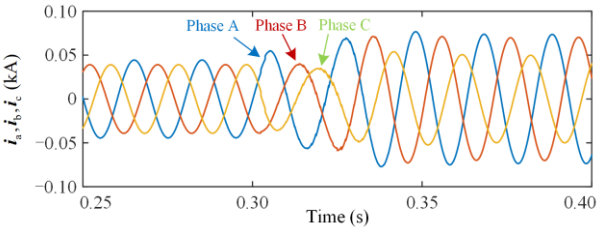


Fig. 10. Current waveform of IIDG2.

Case 1: in islanded mode, a three-phase short-circuit fault occurs at the midpoint of feeder B2C1 at 0.3 s, and the fault resistance is 20 Ω. The phases of the negative-sequence voltage and current fault components are shown in Table II, where the phase differences have been converted to ($0^{o}$, $180^{o}$).

As shown in Table II, the phase difference of A3 is 127°, and that of B1 at the other terminal of the feeder is 61°. The phase differences at these two terminals are in different ranges, indicating that A3B1 is a non-fault feeder. For the feeder B2C1, the phase difference of B2 is 151°, and that of C1 is 113°. It satisfies the fault detection criterion, and thus B2C1 is identified as the fault feeder. The same analysis method can be applied to feeder A4D1. As for the branch feeders like B4, C3 and D3, it is difficult to calculate the phase difference of the fault components because of the small changes in cur-

rents. The fault detection criterion cannot be satisfied, and thus these load branch feeders are non-fault feeders.

TABLE II
ELECTRICAL QUANTITIES OF ISLANDED MICROGRID WHEN A THREE-PHASE FAULT OCCURS ON B2C1

| Bus Position | Electrical Quantity | Phase (°) | Phase Difference (°) |
|---|---|---|---|
| Bus A | $\Delta \boldsymbol{u}_{A}$ | 44 | |
| | $\Delta \boldsymbol{i}_{A1}$ | | |
| | $\Delta \boldsymbol{i}_{A2}$ | 120 | 76 |
| | $\Delta \boldsymbol{i}_{A3}$ | −83 | 127 |
| | $\Delta \boldsymbol{i}_{A4}$ | −14 | 58 |
| Bus B | $\Delta \boldsymbol{u}_{B}$ | 38 | |
| | $\Delta \boldsymbol{i}_{B1}$ | 99 | 61 |
| | $\Delta \boldsymbol{i}_{B2}$ | −113 | 151 |
| | $\Delta \boldsymbol{i}_{B3}$ | −16 | 54 |
| | $\Delta \boldsymbol{i}_{B4}$ | | |
| Bus C | $\Delta \boldsymbol{u}_{C}$ | 37 | |
| | $\Delta \boldsymbol{i}_{C1}$ | 150 | 113 |
| | $\Delta \boldsymbol{i}_{C2}$ | −23 | 60 |
| | $\Delta \boldsymbol{i}_{C3}$ | | |
| Bus D | $\Delta \boldsymbol{u}_{D}$ | 43 | |
| | $\Delta \boldsymbol{i}_{D1}$ | 165 | 122 |
| | $\Delta \boldsymbol{i}_{D2}$ | −8 | 51 |
| | $\Delta \boldsymbol{i}_{D3}$ | | |

Case 2: In grid-connected mode, a phase A-to-phase B short-circuit fault occurs at 0.3 s at the midpoint of feeder A4D1, and the fault resistance is 20 Ω. The phases of the negative-sequence voltage and current fault components are shown in Table III.

TABLE III
ELECTRICAL QUANTITIES OF GRID-CONNECTED MICROGRID WHEN A PHASE-TO-PHASE FAULT OCCURS ON A4D1

| Bus Position | Electrical Quantity | Phase (°) | Phase Difference (°) |
|---|---|---|---|
| Bus A | $\Delta \boldsymbol{u}_{A}$ | −73 | |
| | $\Delta \boldsymbol{i}_{A1}$ | 56 | 129 |
| | $\Delta \boldsymbol{i}_{A2}$ | −121 | 48 |
| | $\Delta \boldsymbol{i}_{A3}$ | −156 | 83 |
| | $\Delta \boldsymbol{i}_{A4}$ | −123 | 50 |
| Bus B | $\Delta \boldsymbol{u}_{B}$ | −74 | |
| | $\Delta \boldsymbol{i}_{B1}$ | 24 | 98 |
| | $\Delta \boldsymbol{i}_{B2}$ | −156 | 82 |
| | $\Delta \boldsymbol{i}_{B3}$ | −149 | −75 |
| | $\Delta \boldsymbol{i}_{B4}$ | | |
| Bus C | $\Delta \boldsymbol{u}_{C}$ | −85 | |
| | $\Delta \boldsymbol{i}_{C1}$ | 24 | 109 |
| | $\Delta \boldsymbol{i}_{C2}$ | −150 | 65 |
| | $\Delta \boldsymbol{i}_{C3}$ | | |
| Bus D | $\Delta \boldsymbol{u}_{D}$ | −73 | |
| | $\Delta \boldsymbol{i}_{D1}$ | 2 | 75 |
| | $\Delta \boldsymbol{i}_{D2}$ | −133 | 60 |
| | $\Delta \boldsymbol{i}_{D3}$ | 105 | 178 |

As shown in Table III, for the feeder A3B1, the phase difference of A3 is 83° and that of B1 is 98°, which means A3B1 is a non-fault feeder. The same analysis method can be applied to the feeder B2C1. As for the feeder A4D1, the phase differences at both terminals are in the same phase range of 0° to 90°, and thus, A4D1 is the fault feeder.

Case 3: In islanded mode, a phase A-to-phase C short-circuit fault occurs on feeder D3 at 0.3 s, and the fault resistance is 20 Ω. The phases of the negative-sequence voltage and current fault components are shown in Table IV.

TABLE IV
ELECTRICAL QUANTITIES OF ISLANDED MICROGRID WHEN A PHASE-TO-PHASE FAULT OCCURS ON D3

| Bus Position | Electrical Quantity | Phase (°) | Phase Difference (°) |
|---|---|---|---|
| Bus A | $\Delta \boldsymbol{u}_{A}$ | −163 | |
| | $\Delta \boldsymbol{i}_{A1}$ | | |
| | $\Delta \boldsymbol{i}_{A2}$ | −82 | 81 |
| | $\Delta \boldsymbol{i}_{A3}$ | 44 | 153 |
| | $\Delta \boldsymbol{i}_{A4}$ | 120 | 77 |
| Bus B | $\Delta \boldsymbol{u}_{B}$ | −166 | |
| | $\Delta \boldsymbol{i}_{B1}$ | −133 | 33 |
| | $\Delta \boldsymbol{i}_{B2}$ | 22 | 172 |
| | $\Delta \boldsymbol{i}_{B3}$ | 124 | 70 |
| | $\Delta \boldsymbol{i}_{B4}$ | 7 | 173 |
| Bus C | $\Delta \boldsymbol{u}_{C}$ | −167 | |
| | $\Delta \boldsymbol{i}_{C1}$ | −157 | 10 |
| | $\Delta \boldsymbol{i}_{C2}$ | 55 | 138 |
| | $\Delta \boldsymbol{i}_{C3}$ | 10 | 177 |
| Bus D | $\Delta \boldsymbol{u}_{D}$ | −175 | |
| | $\Delta \boldsymbol{i}_{D1}$ | −70 | 105 |
| | $\Delta \boldsymbol{i}_{D2}$ | 121 | 64 |
| | $\Delta \boldsymbol{i}_{D3}$ | 100 | 85 |

As shown in Table IV, for the double-terminal feeders A3B1, B2C1 and A4D1, the phase differences at the corresponding two terminals are in different phase ranges, which indicates that they are non-fault feeders. For the load branch feeders B4, C3 and D3, the phase differences of B4 and C3 are in the range of 90° to 180°, and thus B4 and C3 are also non-fault feeders. As for feeder D3, the phase difference is 85°, which means it can be identified as the fault feeder.

Case 4: In grid-connected mode, a phase A-to-phase B short-circuit fault occurs at the midpoint of feeder B2C1 at 0.3 s, and the fault resistance is 50 Ω. The phases of the negative-sequence voltage and current fault components are shown in Table V.

As shown in Table V, for the double-terminal feeders A3B1 and A4D1, the phase differences at the two terminals are in different phase ranges, which indicates that they are non-fault feeders. As for B2C1, the phase differences at the two terminals are in the same phase range. Thus, the fault feeder B2C1 can be located.

Compared with Case 1, the microgrid in Case 4 operates in the grid-connected mode, and DG1 adopts the proposed fault control strategy. Even if the fault resistances are different with different fault types, the fault feeder B2C1 can be identified in both islanded and grid-connected modes.

TABLE V
ELECTRICAL QUANTITIES OF GRID-CONNECTED MICROGRID WHEN A PHASE-TO-PHASE FAULT OCCURS ON B2C1

| Bus Position | Electrical Quantity | Phase (°) | Phase Difference (°) |
|---|---|---|---|
| Bus A | $\Delta \boldsymbol{u}_{A}$ | −73 | |
| | $\Delta \boldsymbol{i}_{A1}$ | 54 | 127 |
| | $\Delta \boldsymbol{i}_{A2}$ | 59 | 132 |
| | $\Delta \boldsymbol{i}_{A3}$ | −127 | 54 |
| | $\Delta \boldsymbol{i}_{A4}$ | −127 | 54 |
| Bus B | $\Delta \boldsymbol{u}_{B}$ | −76 | |
| | $\Delta \boldsymbol{i}_{B1}$ | 54 | 130 |
| | $\Delta \boldsymbol{i}_{B2}$ | −126 | 50 |
| | $\Delta \boldsymbol{i}_{B3}$ | −139 | 63 |
| | $\Delta \boldsymbol{i}_{B4}$ | 87 | 163 |
| Bus C | $\Delta \boldsymbol{u}_{C}$ | −76 | |
| | $\Delta \boldsymbol{i}_{C1}$ | 10 | 86 |
| | $\Delta \boldsymbol{i}_{C2}$ | −140 | 64 |
| | $\Delta \boldsymbol{i}_{C3}$ | 103 | 179 |
| Bus D | $\Delta \boldsymbol{u}_{D}$ | −75 | |
| | $\Delta \boldsymbol{i}_{D1}$ | 38 | 113 |
| | $\Delta \boldsymbol{i}_{D2}$ | −137 | 62 |
| | $\Delta \boldsymbol{i}_{D3}$ | | |

Case 5: In grid-connected mode, a three-phase short-circuit fault occurs at the midpoint of feeder A4D1 at 0.3 s, and the fault resistance is 50 Ω. The phases of the negative-sequence voltage and current fault components are shown in Table VI.

As shown in Table VI, for the double-terminal feeders A3B1 and B2C1, the phase differences at the two terminals are in different phase ranges, which indicates that they are non-fault feeders. As for A4D1, the phase differences at the two terminals are in the same phase range. Thus, the fault feeder A4D1 can be located.

TABLE VI
ELECTRICAL QUANTITIES OF GRID-CONNECTED MICROGRID WHEN A THREE-PHASE FAULT OCCURS ON A4D1

| Bus Position | Electrical Quantity | Phase (°) | Phase Difference (°) |
|---|---|---|---|
| Bus A | $\Delta \boldsymbol{u}_{A}$ | −63 | |
| | $\Delta \boldsymbol{i}_{A1}$ | 57 | 120 |
| | $\Delta \boldsymbol{i}_{A2}$ | −121 | 58 |
| | $\Delta \boldsymbol{i}_{A3}$ | −124 | 61 |
| | $\Delta \boldsymbol{i}_{A4}$ | −147 | 84 |
| Bus B | $\Delta \boldsymbol{u}_{B}$ | −63 | |
| | $\Delta \boldsymbol{i}_{B1}$ | 56 | 119 |
| | $\Delta \boldsymbol{i}_{B2}$ | −123 | 60 |
| | $\Delta \boldsymbol{i}_{B3}$ | −121 | 58 |
| | $\Delta \boldsymbol{i}_{B4}$ | | |
| Bus C | $\Delta \boldsymbol{u}_{C}$ | −64 | |
| | $\Delta \boldsymbol{i}_{C1}$ | 57 | 121 |
| | $\Delta \boldsymbol{i}_{C2}$ | −122 | 58 |
| | $\Delta \boldsymbol{i}_{C3}$ | | |
| Bus D | $\Delta \boldsymbol{u}_{D}$ | −64 | |
| | $\Delta \boldsymbol{i}_{D1}$ | 20 | 84 |
| | $\Delta \boldsymbol{i}_{D2}$ | −121 | 58 |
| | $\Delta \boldsymbol{i}_{D3}$ | | |

Compared with Case 1, the microgrid in Case 5 operates in grid-connected mode, and DG1 adopts the proposed fault control strategy. During the symmetrical faults, the fault feeder can be identified in both islanded and grid-connected modes. Compared with Case 2, the proposed coordinating control and protection scheme is applicable to both symmetrical and asymmetrical faults.

## VI. DISCUSSION

Traditional protection schemes are designed for SG-based distribution networks. Some enhanced protection schemes which adjust the protection thresholds through intelligent algorithms to adapt to the IIDG-dominated microgrids have been studied. However, when the microgrid topology and grid code change, the protection schemes and their thresholds need to be re-tuned. Traditional protection schemes and their enhanced versions ignore the controllability of IIDGs. Therefore, by taking LVRT, grid code and fault control all into consideration, the coordinating fault control and protection strategy is the most promising state-of-the-art technology.

The proposed coordinating control and protection scheme is able to protect a microgrid in all operational modes under all types of faults with improved reliability. The positive- and negative-sequence currents are controlled independently for voltage support and fault characteristic generation. Since the proposed fault detection method is based on steady-state fault characteristics, relays do not require high-speed communication networks. The fault detection method is designed based on the specific negative-sequence fault characteristics, and therefore, when the positive-sequence LVRT control strategy or grid code changes, there is no need to redesign the protection scheme for the microgrid. Although some studies [24]–[26] have begun to focus on IIDGs to generate fault characteristics, these control strategies lack consideration of the coordination between fault characteristic generation and voltage support.

The proposed fault control strategy is designed for inertia-free IIDGs. Therefore, it is not applicable to IIDGs with inertia such as virtual synchronous generators (VSGs), Type-3 wind turbine generators, etc. In addition, with a symmetrical fault inception, it takes an additional cycle for IIDGs to generate fault characteristics.

## VII. CONCLUSION

A sequence component current-based fault control strategy, which makes the fault component protection principle applicable to a microgrid, is proposed in this paper. A new microgrid fault detection method based on negative-sequence fault component is presented. The voltage support and fault characteristics generation of IIDGs are comprehensively considered. During LVRT, the positive-sequence control can flexibly support the microgrid voltage according to different grid codes. From

the fault control strategy of IIDGs, the fault models of a microgrid can be improved. Specific negative-sequence fault characteristics can be generated or enhanced under symmetrical or asymmetrical faults. Without complicated calculation, protection relays can locate the fault feeder accurately by analyzing the phase relationship between the negative-sequence voltage and current fault components. Based on the fault control strategy, the fault detection method can deal with all types of faults in both grid-connected and islanded microgrids. The proposed fault control strategy and fault detection method make full use of the coordination of IIDGs' control and microgrid protection. Simulation results validate the correctness of the fault control strategy and the effectiveness of the microgrid fault detection method.

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## AUTHORS' CONTRIBUTIONS

Zihao Wang: conceptualization, methodology, writing original draft. Longhua Mu: reviewing and editing, supervision, and funding acquisition. Both authors read and approved the final manuscript.

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## AVAILABILITY OF DATA AND MATERIALS

Not applicable.

## DECLARATIONS

Competing interests: The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this article.

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