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Discrete space vector modulation and optimized switching sequence model predictive control for three-level voltage source inverters

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Abstract

This paper proposes a discrete space vector modulation and optimized switching sequence model predictive controller for three-level neutral-point-clamped inverters in grid-connected applications. The proposed strategy is based on cascaded model predictive control (MPC) for controlling the grid current while maintaining the capacitor voltage balanced without weighting factor. To enhance the closed-loop performance, the external MPC evaluates 19 basic and 138 virtual vectors (VV) of the proposed space vector method. The optimal control voltage is then selected using an extended deadbeat method to reduce the execution time of the proposed control algorithm. By using the discrete space vector modulation principle, the VV are synthesized based on switching sequence (SS) and are divided into negative and positive SSs considering their impact on the neutral point (NP) potential. The inner MPC evaluates both types of SSs and selects the one that keeps the capacitor voltage balanced. Various controllers are evaluated and compared against the proposed control strategy. The results show that the proposed strategy improves performance without weighting factor, while maintaining a total harmonic distortion of current to be less than 2%. Compared to the modulated MPC which provides the same fixed switching frequency, the proposed controller reduces the computational burden by over 50% while also providing better NP voltage balance accuracy.

Keywords Three-level inverter, Fixed switching frequency, Model predictive control (MPC), Optimal switching sequence (OSS), Discrete space vector modulation (DSVM)

1 Introduction

Energy shortage and environmental pollution have become critical concerns. This has led to an increased focus on the development of renewable energy sources. As numerous new energy generation systems and flexible AC transmission devices are integrated into the grid, inverters have become an indispensable part of energy conversion systems [1]. In comparison to two-level inverters, the 3L-NPC voltage source inverters boast advantages such as lower output harmonics and reduced semiconductor voltage stress [2, 3]. Consequently, they have been widely adopted in many product lines in renewable energy systems. In addition, the advance of microprocessor technology has enabled the implementation of novel and computationally intensive control algorithms for power electronic topologies and electrical drives, such as predictive control [4]. Such control

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algorithms often have higher computational requirement than the traditional PI-type controllers [5, 6]. Among these control strategies, the most prominent ones include deadbeat, lag-based, trajectory-based and model predictive control.

For classic finite control-set model predictive control (FCS-MPC) [7], optimal control actions are obtained by predicting system behavior and evaluating cost functions over all possible states of the converter [8, 9]. FCS-MPC offers advantages such as fast dynamic response, simplicity in handling nonlinearity and constraints, and a multivariable control approach [10, 11]. Nevertheless, its main drawbacks include the short sampling time requirement, variable switching frequency and high computation time. These limit its application in multi-level converters [12, 13]. To apply to three-level inverters, the classic FCS-MPC needs to evaluate 27 virtual vectors (VV) in each control cycle, resulting in poor THD performance and significant current ripple [14]. It also entails a high computational workload, posing a challenge for its implementation on DSP/FPGA control hardware. In the case of 3L-NPC inverters, MPC employs current and capacitor voltage control objectives for closed-loop control, whose performance is influenced by the weighting factors (WFs) [15, 16]. The selected WFs establish the trade-off between current accuracy and capacitor voltage control, with higher WF values reducing current accuracy and lower values increasing neutral point (NP) voltage imbalance. WF selection often relies on empirical methods, incurring a significant amount of time. Also, classic FCS-MPC results in variable switching frequency, which complicates the design of filters [17, 18].

Many researchers have made improvements to the FCS-MPC strategy to address the above issues. Regarding the tuning of WFs, references [19] and [20] use fuzzy methods and neural networks to obtain the best WF solution for each operating condition, respectively. In [21], a fast finite switching state MPC without WF is proposed, where the selected voltage vectors are used for tracking the current reference and the redundant vectors for balancing the DC capacitance voltage. However, the method is less effective because of the limited number of states used to control NP voltage.

To address the issue of variable switching frequency in the MPC strategies, a digital filter is employed in [22–24] to narrow the switching frequency to a specific range. In [25], an artificial intelligence method is proposed for online tuning of the WFs and regulating the average switching frequency. Reference [26] proposes a modulated MPC (M^2PC) strategy to realize capacitor voltage balance by controlling the duty cycle of redundant vectors. However, this method has the drawback of imposing a high computational burden and is of limited applicability. An effective method to resolve the issue of variable switching frequency in MPC strategies is to seek an optimal switching sequence (OSS) instead of a single switching state per control period. In [27], six local OSSs are considered and evaluated in the power control objectives to determine the global OSS for the next sample, whereas in [28], OSS-MPC based on two cost functions is proposed to independently control current and capacitor voltages without WF. However, this method needs to compute the solution of the relaxation problem first, followed by the use of non-negative constraints to solve the OSS, resulting in a high computational burden. Li et al. [29] introduces the use of a cost function to define the region with the OSS candidates for evaluation, thereby reducing the computational burden. However, the execution time is still quite high because of the need to calculate the duty cycle corresponding to the OSS. To further reduce the execution time, the deadbeat control technique is proposed to select the required control voltage without evaluation of the voltage control objective [30, 31]. In [32], deadbeat-predictive torque control with discrete space-vector modulation is proposed to reduce the torque ripple and the computational burden of the conventional predictive torque control method. Nevertheless, a control method that can achieve high control precision while simultaneously addressing the challenges related to the absence of WF, fixed switching frequency, and low computational burden still requires further research and development.

In this paper, a discrete space vector modulation and optimized switching sequence model predictive controller (DSVM-OSS-MPC) strategy is proposed. The main contributions of this paper include the following three aspects:

(1) Controlling grid current based on the cascade MPC while maintaining capacitor voltage balance without WF, thus eliminating the cost of WF selection.
(2) Achieving superior current tracking accuracy and NP voltage balance. To improve the closed-loop performance, DSVM is used to achieve a new space vector with 157 voltage vectors instead of the 19 basic vectors used in classic MPC. The additional 138 vectors are virtual and synthesized using the OSS which considers the impact of each vector on NP voltage and the reduction of switching commutation.
(3) Significantly reduced computational burden is achieved. To avoid the exhaustive search for the optimal control solution among the 157 SS candidates, the extended deadbeat method is used in the outer MPC to reduce the closed-loop control to a sub-optimal problem. The inner MPC then focuses

on the redundant SSs to select the optimal solution. Therefore, the proposed control strategy offers the benefit of delivering accurate current response and maintaining capacitor voltage balance, while simultaneously exhibiting characteristics of no WF influence and reduced computational burden.

The rest of this paper is organized as follows: the classic MPC method is presented in Sect. 2, while Sect. 3 introduces the basic principles of switching sequence MPC. Section 4 provides a detailed description of the proposed DSVM-OSS-MPC, including the extension of the space vector based on the DSVM and OSS, the selection method of the optimum voltage vector, and the optimization of the capacitor voltage balance. In Sect. 5, experiments and simulations are carried out to verify the effectiveness and superiority of DSVM-OSS-MPC. The conclusions are given in Sect. 6.

2 Classic FCS-MPC strategy for 3L-NPC

Figure 1 presents a 3L-NPC inverter connected to the grid. The DC-side of the converter consists of two capacitors supplied by a DC voltage v_{dc}. At the AC-side, the converter is connected to the three-phase sources (e_{a}, e_{b}, e_{c}) through the RL filter and injects three-phase currents (i_{a}, i_{b}, i_{c}) to the grid. Each phase of the three-level NPC consists of four switches S_{xi} with $x \in \{a, b, c\}$ and $1 \leq \mathrm{i} \leq 4$, and generates up to three switching levels $S_x \in \{-1, 0, 1\}$. Considering the three legs, the inverter can generate 27 switching states $S_{j\mathrm{abc}}$.

with $1 \leq j \leq 27$. To obtain the optimal state for the next sample with the MPC, the dynamic response of the system due to each switching state candidate $S_{j\mathrm{abc}}$ is predicted and evaluated.

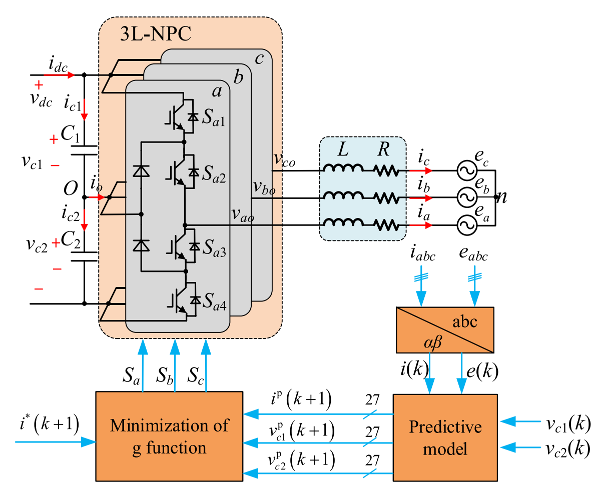

Fig. 1 Grid-connected 3L-NPC converter and flow diagram of the classic FCS-MPC strategy

From the modeling approach described in [33] and considering the variables given in Table 1, the grid currents, and the sum and difference in the dynamics of the DC-link voltage in the $\alpha\beta\gamma$ reference frame can be expressed as:

$$L\frac{d}{dt}i_{\alpha\beta} = \frac{1}{2}x_1 S_{\alpha\beta} + \begin{bmatrix} \frac{1}{2\sqrt{6}}\left(S_\beta^2 - S_\alpha^2\right) - \frac{1}{\sqrt{3}}S_\alpha S_\gamma \\ \frac{S_\alpha S_\beta}{\sqrt{6}} - \frac{S_\beta S_\gamma}{\sqrt{3}} \end{bmatrix} x_2 - e_{\alpha\beta} - Ri_{\alpha\beta} \tag{1}$$

$$C\dot{x}_1 = -S_{\alpha\beta}^T i_{\alpha\beta} + 2i_{dc} \tag{2}$$

$$C\dot{x}_2 = -\frac{2}{\sqrt{6}}\left[S_\alpha^2 - S_\beta^2, -S_\alpha S_\beta\right] i_{\alpha\beta} - \frac{1}{\sqrt{6}}S_{\alpha\beta}^T i_{\alpha\beta} S_\gamma \tag{3}$$

where $x_1 = v_{\mathrm{C1}} + v_{\mathrm{C2}}$ and $x_2 = v_{\mathrm{C1}} — v_{\mathrm{C2}}$ are the sum and the difference of the upper and lower DC-link voltages, respectively.

To ensure correct converter operation, x_2 must be near zero or at least one order of magnitude lower than x_1 [33]. In addition, the averaged duty cycle $S_{\alpha\beta}$ is defined within $[-1, 1]$, and therefore the third term located on the right-hand side of (1) can be assumed to be two orders of magnitude lower than the second term. With this consideration, the inductor current dynamics can be approximated by:

$$L\frac{d}{dt}i_{\alpha\beta} = -e_{\alpha\beta} + \mathrm{u} - Ri_{\alpha\beta} \tag{4}$$

where $\mathrm{u} = \frac{1}{2}\, x_1 S_{\alpha\beta}$ is the output voltage vector of the inverter, $i_{\alpha\beta}$ is the output current vector, and $e_{\alpha\beta}$ is the grid voltage vector. From [34], the current predictions at $k+1$ in the $\alpha-$ axis and $\beta-$ axis which are noted as $i_\alpha^p(k+1)$ and $i_\beta^p(k+1)$, are given by:

$$\begin{bmatrix} i_\alpha^p(k+1) \\ i_\beta^p(k+1) \end{bmatrix} = \left(1 - \frac{RT_s}{L}\right)\begin{bmatrix} i_\alpha(k) \\ i_\beta(k) \end{bmatrix} + \frac{T_s}{L}\begin{bmatrix} u_\alpha(k) - e_\alpha(k) \\ u_\beta(k) - e_\beta(k) \end{bmatrix} \tag{5}$$

where i(k) is the measured current at the k sample, while e(k) and u(k) are the measured grid voltage and inverter output voltage at the k sample, respectively.

Table 1 System variables and parameters

Variable	Description
$e_{\alpha\beta} = \{e_\alpha, e_\beta\}^{\mathrm{T}}$	Grid voltage vector in αβγ reference frame
$i_{\alpha\beta} = \{i_\alpha, i_\beta\}^{\mathrm{T}}$	Inductors currents in αβγ reference frame
$S_{\alpha\beta\gamma} = \{S_\alpha, S_\beta, S_\gamma\}^{\mathrm{T}}$	Averaged duty cycles in αβγ reference frame
$v_{\mathrm{C1}}, v_{\mathrm{C2}}$	DC-link capacitors voltages
L, C, R	Smoothing inductor, DC-link capacitor and Line resistance

For NP voltage balance, the capacitor voltages $v_{c1}(k+1)$ and $v_{c2}(k+1)$ related to the capacitors C_1 and C_2 at the $k+1$ sample are predicted as:

$$\begin{bmatrix} v_{c1}^{p}(k+1) \\ v_{c2}^{p}(k+1) \end{bmatrix} = \begin{bmatrix} v_{c1}(k) \\ v_{c2}(k) \end{bmatrix} + \begin{bmatrix} \frac{T_s}{C_1} i_{c1}(k) \\ \frac{T_s}{C_2} i_{c2}(k) \end{bmatrix} \tag{6}$$

where $v_{c1}(k)$ and $v_{c2}(k)$ are the measured capacitor voltages at the k sample. $i_{c1}(k)$ and $i_{c2}(k)$ are the currents flowing through the capacitors at the k sample and are given by:

$$\begin{aligned} i_{c1}(k) &= i_{dc}(k) - \sum_{x=a,b,c} H_{1x} i_x(k) \\ i_{c2}(k) &= i_{dc}(k) + \sum_{x=a,b,c} H_{2x} i_x(k) \end{aligned} \tag{7}$$

where $\mathrm{H}_{1x}=\begin{cases} 1, \text{if } \mathrm{S_x}=1 \\ 0, \text{otherwise} \end{cases}$, and $\mathrm{H}_{2x}=\begin{cases} 1, \text{if } \mathrm{S_x}=-1 \\ 0, \text{otherwise} \end{cases}$.

The standard cost function for tracking the current reference and regulating the capacitor voltage balance is defined in [35], given by:

$$\begin{aligned} g = {} & \left(i_{\alpha}^{*}(k+1) - i_{\alpha}^{p}(k+1)\right)^2 + \left(i_{\beta}^{*}(k+1) - i_{\beta}^{p}(k+1)\right)^2 \\ & + \lambda_{dc}\left(v_{c1}^{p}(k+1) - v_{c2}^{p}(k+1)\right)^2 \end{aligned} \tag{8}$$

where $i_{\alpha}^{*}(k+1)$ and $i_{\beta}^{*}(k+1)$ are the current reference components at instant $k+1$, and λ_{dc} is the WF. For time delay compensation [36], the evaluation of (8), (6), and (5) is considered at $k+2$ rather than $k+1$.

To obtain good performance when using (8), an appropriate trade-off needs to be achieved between tracking current and balancing capacitor voltage. Since λ_{dc} is a function of the operating point and a parameter of the system, the design of λ_{dc} is not trivial [15]. In addition, the unified cost function which provides a single optimal solution does not guarantee that both individual control objectives are optimized [37]. An alternative method to simultaneously track the current and control the capacitor voltages without the need for WF is to use a cascaded MPC approach [15, 37].

3 Basic principle of the SS-MPC

The cascaded SS-MPC approach is proposed in [28] for controlling the grid current and the capacitor voltages of the three-level inverter without the use of WF, as shown in Fig. 2. The outer MPC determines the suboptimal SS candidates which satisfy the current objective, whereas the inner MPC selects between the suboptimal candidates, with the SS ensuring capacitor voltage balance.

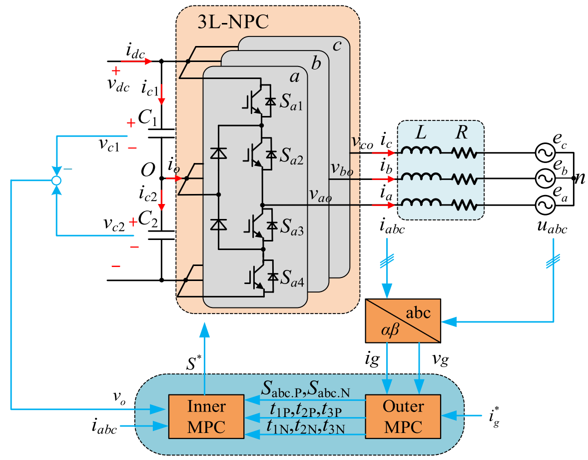

Fig. 2 Grid-connected 3L-NPC converter and flow diagram of the SS-MPC control strategy

Maintaining the capacitor voltages to be balanced requires the control of the NP voltage O, which is defined as $v_o = v_{c2} - v_{c1}$. Considering that the system is balanced and the DC-link voltage is constant, the dynamic *of* v_o is given by:

$$\frac{dv_o(t)}{dt} = \frac{1}{C} i_o(t) \tag{9}$$

The NP current i_o is obtained by:

$$i_o = \left|S_{jabc}\right|^{\mathrm{T}} i_{abc}, \tag{10}$$

where $|\mathrm{S_{jabc}}| = \left[|\mathrm{S_{ja}}|\ |\mathrm{S_{jb}}|\ |\mathrm{S_{jc}}|\right]^{\mathrm{T}}$, and $\mathrm{i_{abc}} = [\mathrm{i_a}, \mathrm{i_b}, \mathrm{i_c}]^{\mathrm{T}}$.

From Fig. 3, the analysis of the 27 switching state candidates of the three-level NPC is divided into four categories of vectors: zero using black dots; small using red dots; medium using blue dots; and larger using green

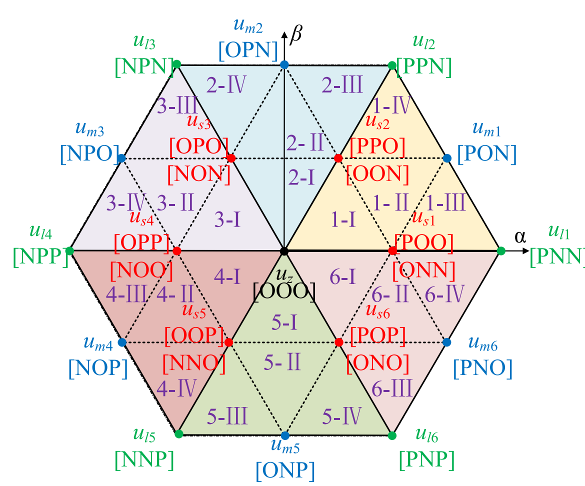

Fig. 3 Grid-connected 3L-NPC converter space vector diagram

Table 2 Classification of small vectors

Type	Switching states (S_{abc})
$S_{abc.P}$	[POO], [PPO], [OPO], [OPP], [OOP], [POP]
$S_{abc.N}$	[ONN], [OON], [NON], [NOO], [NNO], [ONO]

dots. Except for the zero-voltage vectors, only the small vectors can connect the inverter terminals to the same type of DC-link potential. A switching state S_{jabc} is called P-type and noted as $S_{abc.P}$ when only the positive terminal of the DC link is connected to the grid, and N-type $S_{abc.N}$ when connected to the negative terminal. The classification of small vectors according to the type of switching states $S_{abc.P}$ and $S_{abc.N}$ is given in Table 2. Using (10), the direction of NP current can be defined.

For example, by applying the P-type $[O,P,O]^T$ and its associated N-type redundancy $[N,O,N]^T$, the associated NP current according to (10) are $i_o = i_b$ and $i_o = -i_b$, respectively. With an appropriate distribution of several switching combinations within the sampling period, it is possible to control the current as well as NP voltage potential.

The order of the converter applying several S_{jabc} within the control period is known as SS and the controller is called SS-MPC. In PWM and SVM modulation methods, various SS dispositions are reported in the literature. Since SVM is synthesized based on the space vector, it is easier to implement SS-MPC based on SVM than PWM, and it provides a simpler identification of small voltage vectors to control the NP voltage.

To synthesize SVM, the space vector presented in Fig. 3 is divided into six sectors, and each sector is further divided into four regions or sub-sectors. For a 3L-NPC, the total number of regions is 24 and each region has three switching states with one or two small vectors. For instance, region II within sector 1, noted as 1-II, has one medium and two small vectors. Considering SVM based on a symmetric pulse pattern, an SS applied over a control period is given by:

$$S \triangleq \left\{ u_1\left[\frac{t_1}{2}\right], u_2\left[\frac{t_2}{2}\right], u_3[t_3], u_2\left[\frac{t_2}{2}\right], u_1\left[\frac{t_1}{2}\right] \right\} \quad (11)$$

where u_i ($i=1, 2, 3$) is the vector related to the i^{th} switching state of a subset. t_i ($i=1, 2, 3$) is the duration of the i^{th} switching state in a subsection and satisfies the following formula:

$$t_1 + t_2 + t_3 = T_s \quad (12)$$

Focusing on half-sampling time, several dispositions of SS are possible using the vectors u_1, u_2, and u_3. The total number of possible dispositions of switching states in an SS per region increases with the number of redundant vectors. To regroup the SS in each region into two types, the nature of an SS is exclusively defined by the type of its small vectors. For example, in region 1-IV, if a P-type small vector [PPO] is used, the number of possible dispositions of P-type SS are [PON-PPN-PPO], [PON-PPO-PPN] [PPO-PPN-PON], [PPO-PON-PPN], [PPN-PPO-PON] and [PPN-PON-PPO]. In this work, to reduce the switching losses within a control period, the switching effort is restricted. In the first restriction, the switching state per phase (S_x) cannot change between P and N and vice-versa. In the second restriction, only one phase of an applied three-phase switching state (S_{abc}) can change. In such a case, the candidate SSs in subsector 1-IV are PON-PPN-PPO for the P-type and PPN-PON-OON for the N-type. The same principle is used for all the SSs of sector 1 as given in Table 3.

However, the type of the optimal SS, which is applied between two consecutive samples and selected by the inner MPC, can change between the P-type and N-type. For example, considering the previously applied SS of 1-II-P, the next optimal candidate SS selected by the inner MPC is either 1-II-P or 1-II-N if the required control voltage is in sector 1-II. Between two consecutive samples, two phases of the inverter can change. In this scenario, the second restriction is not respected, which will lead to an extra switching effort.

To synthesize the applicable OSS during each sample, the conduction time associated with each switching state within a control period has to be calculated. Various online methods are proposed for obtaining the OSS and the related duty cycle as a function of the resulting current and power errors of the primary term of the cost function [26–29]. Even though they provide an optimal duration candidate for tracking the control objectives, these methods result in a higher computational burden.

Table 3 The switching sequence of sector 1

Sector	Switching sequence type	Switching sequence
1-I	P	OOO-POO-PPO
	N	ONN-OON-OOO
1-II	P	PON-POO-PPO
	N	ONN-OON-PON
1-III	P	PNN-PON-POO
	N	ONN-PNN-PON
1-IV	P	PON-PPN-PPO
	N	OON-PON-PPN

4 Proposed DSVM-OSS-MPC strategy

An offline approach provides an alternative solution to tune the SS candidates without increasing the computational burden of the MPC algorithm. In this paper, DSVM based on virtual vectors is used to synthesize the OSS without the need for the online evaluation of the related switching durations.

4.1 DSVM based on virtual vectors

To improve controller performance, the number of virtual vectors is selected so that the closed-loop performance is similar to the one achieved under MPC-PWM [38]. The virtual vector noted u_v is synthesized by its corresponding SSs as given by:

$$u_v = \sum_{i=1,2,3} d_i u_i \tag{13}$$

$$d_1 + d_2 + d_3 = 1 \tag{14}$$

where u_i is the basic vector and u_v is the virtual vector. d_i is the duty cycle of vector u_i calculated as $d_i = t_i / T_s$. By substituting the coordinates of the three basic and virtual vectors in (13), Eqs. (13) and (14) are developed into a system of three equations. The resulting system is solved offline for obtaining the d_i associated with each u_i.

To expand the number of voltage vectors of sector 1-II from 3 vectors to 6, 10, 19, and 28, the region is further divided as presented in Fig. 4. In [36], the expanded region consists of three actual and three virtual vectors, as shown in Fig. 4a. To select the appropriate extended configuration, the current THD, the average switching frequency (ASF), and the complexity of implementing MPC when n_v increases are considered. To select the suitable expanded region, the MPC with 6, 10, 19, 28 vectors per region are compared with MPC-PWM, as shown in Fig. 5. As seen, when $n_v = 6$, the resulting ASF is lower than that of MPC-PWM, and for a closed-loop control with the lowest ASF and complexity, the suitable configuration is $n_v = 6$. However, the resulting current THD is higher than that under MPC-PWM for the different operating currents.

To achieve a similar current THD as under MPC-PWM, the switching frequency needs to be increased. However, this can be challenging to implement in a low-cost digital processor because of the high computational requirement. For $n_v = 10$, 19, and 28, the resulting current THD and ASF are similar to the values under MPC-PWM. Thus, to obtain performances that are equivalent to the ones achieved under MPC-PWM, the possible candidates are $n_v = 10$, 19, and 28. Considering that for $n_v \in \{10, 19, 28\}$, the improvement of the current THD and the reduction of the ASF are negligible, MPC-DSVM with $n_v = 10$ represents the scenario for achieving a similar closed response to that of MPC-PWM, without imposing excessive implementation complexity.

Considering the case with $n_v = 10$, the expanded space vector is presented in Fig. 6a. Focusing the analysis on the subsector 1-II for instance, the number of virtual vectors synthesized based on three basic vectors is equal to seven as presented in Fig. 6b, and each virtual vector is synthesized according to Table 4. Knowing that a subsector has two types of SS (as seen in Table 3), each virtual vector u_v can be decomposed into P-type and N-type SSs as illustrated in Fig. 7. Hence, the expanded space vector presented in Fig. 6a has a total of 157 vectors divided into 19 basic vectors and 138 virtual vectors. Since the total number of candidate vectors is 6 times the number of states generated by 3L-NPC, it is anticipated that the

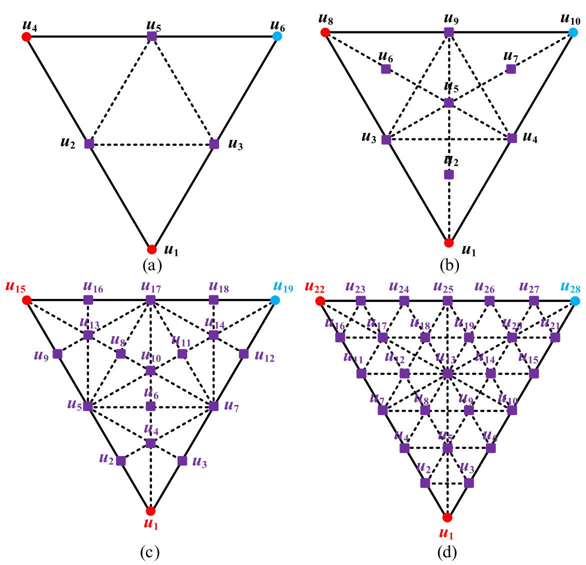

Fig. 4 Subsector 1-II virtual vector arrangement. **a** $n_v = 6$. **b** $n_v = 10$. **c** $n_v = 19$. **d** $n_v = 28$

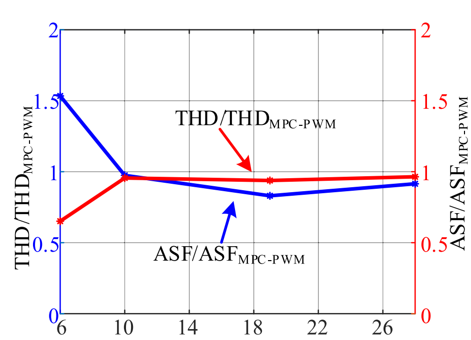

Fig. 5 Current THD and switching frequency change with n_v

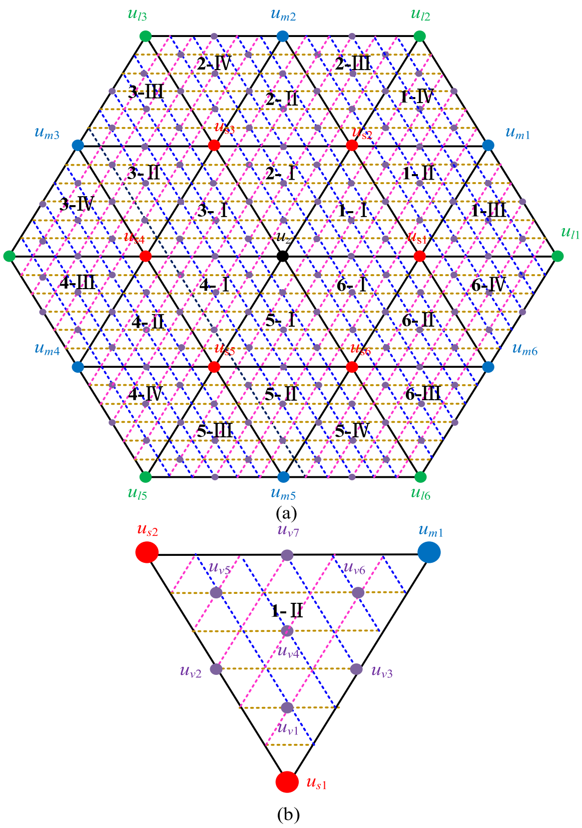

Fig. 6 Proposed extended space vectors. **a** The distribution map of virtual vectors in the expanded space vector. **b** candidate basis and virtual vectors in a region 1-II

Table 4 The synthesis method of virtual vector

Virtual vector	Synthesis method	Virtual vector	Synthesis method
u_v	$d_1u_{s1}+d_2u_{s2}+d_3u_{m1}$	u_{v4}	$\frac{1}{3}u_{s1}+\frac{1}{3}u_{s2}+\frac{1}{3}u_{m1}$
u_{v1}	$\frac{2}{3}u_{s1}+\frac{1}{6}u_{s2}+\frac{1}{6}u_{m1}$	u_{v5}	$\frac{1}{6}u_{s1}+\frac{2}{3}u_{s2}+\frac{1}{6}u_{m1}$
u_{v2}	$\frac{1}{2}u_{s1}+\frac{1}{2}u_{s2}$	u_{v6}	$\frac{1}{6}u_{s1}+\frac{1}{6}u_{s2}+\frac{2}{3}u_{m1}$
u_{v3}	$\frac{1}{2}u_{s1}+\frac{1}{2}u_{m1}$	u_{v7}	$\frac{1}{2}u_{s2}+\frac{1}{2}u_{m1}$

computation time will be excessive when using the classic optimization approach. To implement a control algorithm with a reduced computational burden, it is crucial to reduce the optimization problem to evaluate only the SS candidates which satisfy the optimal control voltage.

4.2 Outer and inner MPCs

To obtain the OSS control action for the next sample, the cost function given in (8) is developed as a function of voltage control objectives. Using the unified optimization method, the cost function is given by:

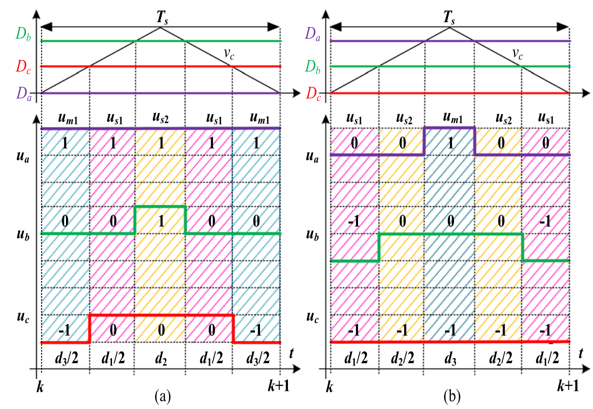

Fig. 7 Type of switching sequences: **a** P-type switching sequence of sub-sector 1- II. **b** N-type switching sequence of sub-sector 1- II

$$g=\left(u_{\alpha}^{*}-u_{v\alpha}\right)^{2}+\left(u_{\beta}^{*}-u_{v\beta}\right)^{2}+\lambda_{dc}\left(v_{o}^{p}(k+1)\right)^{2} \tag{15}$$

$$\begin{bmatrix} u_{\alpha}^{*}(k) \\ u_{\beta}^{*}(k) \end{bmatrix}=\frac{L}{T_s}\begin{bmatrix} i_{\alpha}^{*}(k+1)-i_{\alpha}(k) \\ i_{\beta}^{*}(k+1)-i_{\beta}(k) \end{bmatrix}+R\begin{bmatrix} i_{\alpha}(k) \\ i_{\beta}(k) \end{bmatrix}+\begin{bmatrix} e_{\alpha}(k) \\ e_{\beta}(k) \end{bmatrix} \tag{16}$$

where $u_{\alpha\beta}^{*}(k)$ is the reference voltage components, and v_o is the NP voltage potential given by:

$$v_{o}^{p}(k+1)=\frac{1}{C}\sum_{i=1}^{3}t_i\left(|S_{ia}|i_a+|S_{ib}|i_b+|S_{ic}|i_c\right)+v_o(k) \tag{17}$$

Using the cascaded MPC method, the first primary term of (15) is used by the outer MPC as given by:

$$g_{outer}=\left(u_{\alpha}^{*}-u_{v\alpha}\right)^{2}+\left(u_{\beta}^{*}-u_{v\beta}\right)^{2} \tag{18}$$

The evaluation of (18) requires 157 cycles of calculation which is difficult to achieve, especially with standard digital control processors. To obtain the optimal vector with the lowest computational requirement, an extended deadbeat method is developed. The main idea is to define the boundaries associated with each candidate voltage vector in the expanded space vector, and use the coordinates of the reference to identify the region which is associated with the optimal control action.

Considering sector 1 in Fig. 6a, the vectors are projected in the reference formed by the three axes L_1, L_2, and L_3 as illustrated in Fig. 8. As seen, L_1 is parallel to the axis noted as [ONN-PPN], L_2 is parallel to the axis noted as [OOO-PON], and L_3 is parallel to the axis noted as [PNN-PPO]. It can also be seen from Fig. 8 that each virtual vector is the center of a smaller

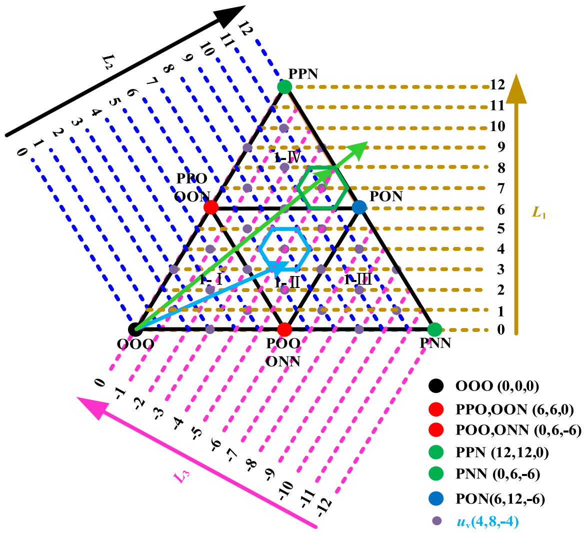

Fig. 8 Schematic diagram of optimized voltage vector selection

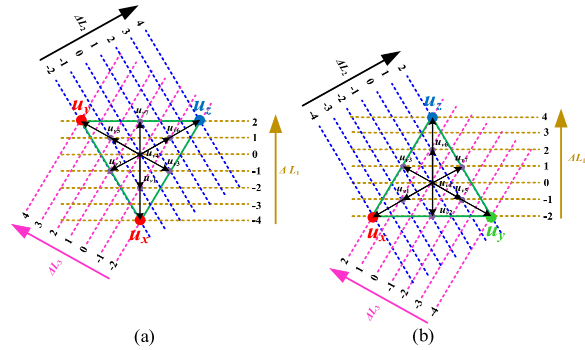

Fig. 9 Type of subsectors or regions: **a** A type. **b** B type

hexagon, i.e., the region defined by each small hexagon corresponds to a given optimal voltage vector. Assuming that the reference voltage vector is u^* as represented by the light blue vector in Fig. 8, the virtual vector u_v which is the center of the light blue hexagon is the optimal control voltage.

In general, the coordinates of the reference vector are given by:

$$L_1 = \frac{12\sqrt{3}u_\beta^*(k)}{V_{dc}} \tag{19}$$

$$L_2 = \frac{18u_\alpha^*(k) + 6\sqrt{3}u_\beta^*(k)}{V_{dc}} \tag{20}$$

$$L_3 = \frac{6\sqrt{3}u_\beta^*(k) - 18u_\alpha^*(k)}{V_{dc}} \tag{21}$$

In the case where the reference vector u^* exceeds the maximum modulation range, u^* is scaled back into the converter operating region as illustrated by the green vector in Fig. 8 and is given by:

$$u^*(k) = \begin{cases} u^*(k)\frac{|u_{\max}|}{|u^*(k)|}, & |u^*(k)| > |u_{\max}| \\ u^*(k) & \text{otherwise} \end{cases} \tag{22}$$

where $|u_{\max}|$ is the module of the maximum voltage vector.

With the coordinates of the reference voltage, two steps are needed to determine the optimal control voltage. The first step is to localize the smaller sector and the second is to find the corresponding smaller hexagon. For the first step, each small sector is defined by the boundary conditions in three axes. For example, the voltage reference is within the small sector 1-II, if $L_1 \le 6$, $L_2 \ge 6$, and $L_3 \ge -6$. The second step is to determine the small hexagon with the small vector adjacent to the vector reference. It should be noted that two dispositions of small sectors are possible in a sector, and the distribution of virtual vectors depends on the type of disposition as presented in Fig. 9. The error, ΔL, between the reference voltage and the center of a given small sector is defined by:

$$\begin{bmatrix} \Delta L_1 \\ \Delta L_2 \\ \Delta L_3 \end{bmatrix} = \begin{bmatrix} L_1(u^*) \\ L_2(u^*) \\ L_3(u^*) \end{bmatrix} - \begin{bmatrix} L_1(u_{\text{center}}) \\ L_2(u_{\text{center}}) \\ L_3(u_{\text{center}}) \end{bmatrix} \tag{23}$$

where $L_1(u^*)$, $L_2(u^*)$, and $L_3(u^*)$ are the coordinates of u^* on L_1, L_2, and L_3, respectively. $L_1(u_{\text{center}})$, $L_2(u_{\text{center}})$, and $L_3(u_{\text{center}})$ are the coordinates of u_{center} on L_1, L_2, and L_3 respectively. When the reference voltage is adjacent to an actual vector, u_x, u_y or u_z, the new center used to evaluate (23) is associated with a small sector and is given by $u_{\text{center}} = (u_x + u_y + u_z)/3$. In summary, the rules for selecting the optimal control voltage are given in Table 5.

Taking u^* represented in Fig. 8 as an example, with the coordinates $L_1 = 3.6$, $L_2 = 7.3$, and $L_3 = -4.5$, u^* belongs to sector 1− II which is an A-type disposition. The adjacent center to the reference control voltage is obtained by rounding up u^* and the resulting coordinates are (4, 8, -4). With the coordinates of u^* and u_{center}, ΔL is (-0.4, -0.7, -0.5). From Table 5, the optimal voltage vector is u_{v4}, which is synthesized by applying u_x, u_y, and u_z during the duty cycles 1/3, 1/3, and 1/3, respectively.

The optimal voltage control provided by the outer MPC is used by the inner controller for the NP voltage balance. The cost function of the inner loop is defined as:

Table 5 Rules for selecting the optimal control voltage

The output voltage vector	boundaries		Duty cycle		
	A type	B type	d_{ux}	d_{uy}	d_{uz}
u_x	$\Delta L_1 \le -3$	$\Delta L_2 \le -3$	1	0	0
u_y	$\Delta L_3 \ge 3$	$\Delta L_3 \le -3$	0	1	0
u_z	$\Delta L_2 \ge 3$	$\Delta L_1 \ge 3$	0	0	1
u_{v1}	$-3<\Delta L_1 \le -1$ $\Delta L_2 \le 0$ $\Delta L_3 \le 0$	$\Delta L_1 \le 0$ $-3<\Delta L_2 \le -1$ $0<\Delta L_3$	2/3	1/6	1/6
u_{v2}	$\Delta L_1 \le 0$ $\Delta L_2 \le -1$ $0<\Delta L_3$	$\Delta L_1 \le -1$ $\Delta L_2 < 0$ $\Delta L_3 \le 0$	1/2	1/2	0
u_{v3}	$\Delta L_1 \le 0$ $0<\Delta L_2$ $\Delta L_3 \le -1$	$0<\Delta L_1$ $\Delta L_2 \le 0$ $1<\Delta L_3$	1/2	0	1/2
u_{v4}	$-1<\Delta L_1<1$ $-1<\Delta L_2<1$ $-1<\Delta L_3<1$	$-1<\Delta L_1<1$ $-1<\Delta L_2<1$ $-1<\Delta L_3 \le 1$	1/3	1/3	1/3
u_{v5}	$0<\Delta L_1$ $\Delta L_2 \le 0$ $1 \le \Delta L_3<3$	$\Delta L_1 \le 0$ $0 \le \Delta L_2$ $-3 \le \Delta L_3 \le -1$	1/6	2/3	1/6
u_{v6}	$0<\Delta L_1$ $1 \le \Delta L_2<3$ $\Delta L_3 \le 0$	$1 \le \Delta L_1<3$ $0<\Delta L_2$ $0<\Delta L_3$	1/6	1/6	2/3
u_{v7}	$1 \le \Delta L_1$ $0<\Delta L_2$ $0<\Delta L_3$	$0<\Delta L_1$ $1 \le \Delta L_2$ $\Delta L_3 \le 0$	0	1/2	1/2

$$g_{inner} = \left[\frac{1}{C} \sum_{i=1}^{3} t_i(|S_{ia}|i_a + |S_{ib}|i_b + |S_{ic}|i_c) + v_o(k) \right]^2 \tag{24}$$

The optimal vector can be either a basic or virtual vector, and so is selected from the 157 vectors. In the case where it is a virtual vector, the inner MPC selects the type of SS that ensures a better NP voltage balance. The proposed DSVM-OSS-MPC uses the whole extended space vector with 157 compared to 19 for the classic MPC, and therefore a better current accuracy can be achieved.

The block diagram of the proposed strategy is shown in Fig. 10 and the algorithm is described by the following main steps.

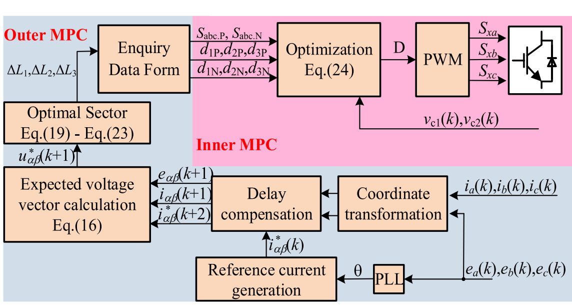

Fig. 10 DSVM-OSS-MPC control block diagram

(1) Measure $i_{\alpha\beta}(k)$, $e_{\alpha\beta}(k)$, $v_{c1}(k)$ and $v_{c2}(k)$.
(2) Apply the optimal switching sequence.
(3) Predict $i_{\alpha\beta}(k+1)$, $e_{\alpha\beta}(k+1)$, $i^*_{\alpha\beta}(k+2)$, and $u^*_{\alpha\beta}(k+2)$.
(4) Calculate L_1, L_2, and L_3 associated to $u^*_{\alpha\beta}(k+2)$.
(5) Use the coordinates of $u^*_{\alpha\beta}(k+2)$ to select $u_{\alpha\beta}(k+2)$.
(6) Select N- or P-type SS which minimizes g_{inner}.

5 Simulation and experimental results

For validation purposes, the effectiveness of the proposed controller is compared with the classic MPC [33], the FS-MPC without WF (WMPC) [21], and the M^{2}PC [26]. The parameters of the system used for the evaluation are given in Table 6 and the controller operating sampling frequency is 10 kHz.

Table 6 System parameters

	Parameter	Grid-Connected	
		Simulation	Experimental
V_{dc}	DC-link voltage	800 V	110 V
E_m	Line-line voltage (RMS)	380V	50 V
C	DC link capacitors	500 μF	2200 μF
f	Fundamental frequency	50 Hz	50 Hz
R	Resistance	0.1 Ω	0.5 Ω
I_{ref}	Reference current	15/30 A	3/6 A
L	Filter inductance	5 mH	7 mH

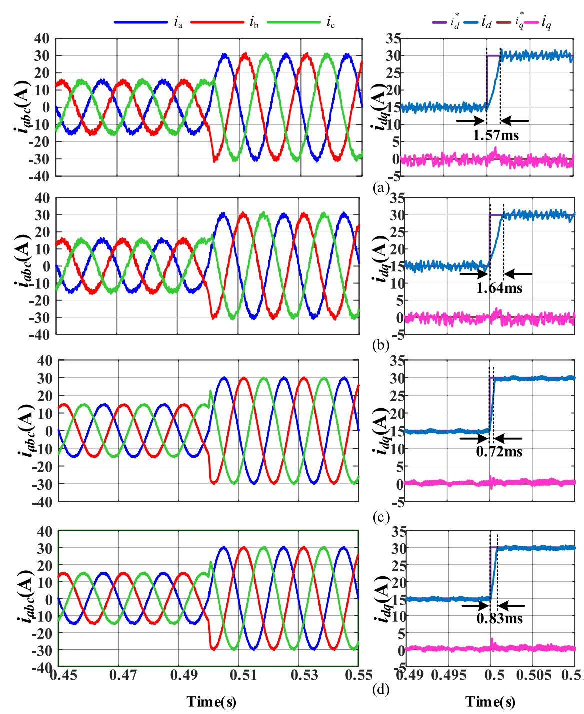

Fig. 11 Comparative evaluation of the current response. **a** Classic MPC. **b** WMPC. **c** M^{2}PC. **d** DSVM-OSS-MPC

5.1 Simulation results and discussion

The comparative evaluation of the four control strategies with a current step change from 15 to 30A is presented in Figs. 11, 12. As seen from Fig. 11 M^2PC provides the fastest response with a time response $t_{s(c)} = 0.72$ ms, i.e. faster than $t_{s(d)} = 0.83$ ms with the proposed controller. However, compared to the respective response times of $t_{s(a)} = 1.57$ ms and $t_{s(b)} = 1.64$ ms with MPC and WMPC, the proposed DSVM-OSS-MPC presents a faster dynamic response.

From Fig. 12, with both 15 A and 30 A operating currents, the NP voltage with classic MPC and WMPC is higher with a value equal $v_{o(a)} = 9.2$ V and $v_{o(b)} = 8.2$ V, respectively. While the proposed strategy and M^2PC ensure a better balanced capacitor voltage with the peak NP voltages of $v_{o(c)} = 5.3$ V and $v_{o(d)} = 5.2$ V, respectively.

To provide a fair comparison on the steady-state performances of different control methods, the four controllers are operated at the same ASF. The ASF of a 3L-NPC inverter is defined as

$$\mathrm{ASF} = \frac{1}{12} \sum_{n=a,b,c} \sum_{i=1}^{4} \mathrm{ASF}_{ni} \tag{25}$$

where ASF_{ni} denotes the switching times of the ith IGBT of n-phase in one second.

The comparative evaluation of the four control strategies is made with a similar resulting ASF (2 kHz) and the results are presented in Figs. 13 and 14, where the sampling frequencies of the classic MPC, WMPC, M^2PC and DSVM-OSS-MPC are 15 kHz, 15 kHz, 6 kHz, and 6 kHz, respectively. It can be noted that the four control strategies provide similar output current THD when operating at a similar average switching frequency. The current THD with classic MPC, WMPC, M^2PC and DSVM-OSS-MPC are $\mathrm{THD}_{(a)} = 2.15\%$, $\mathrm{THD}_{(b)} = 2.16\%$, $\mathrm{THD}_{(c)} = 2.32\%$, and $\mathrm{THD}_{(d)} = 2.31\%$, respectively. However, compared to MPC and WMPC, both the proposed controller and M^2PC strategies operate at a fixed switching frequency of 6 kHz.

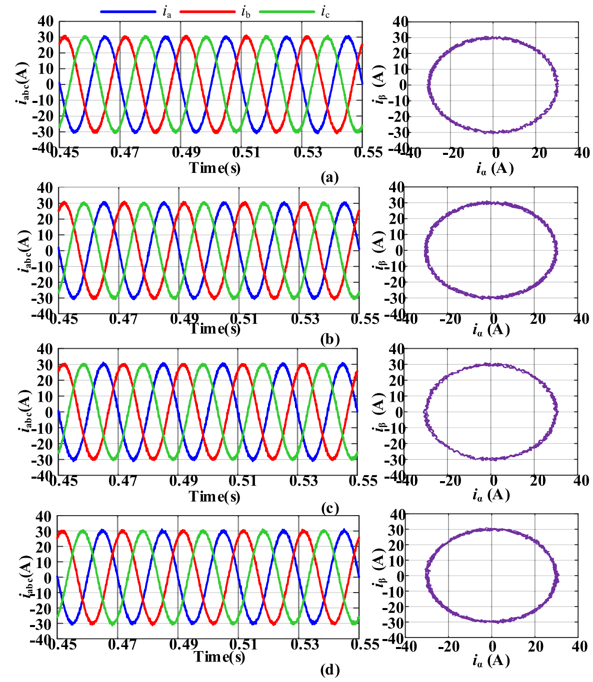

Fig. 13 Comparative evaluation of the steady state current response. **a** Classic MPC. **b** WMPC. **c** M^2PC. **d** DSVM-OSS-MPC

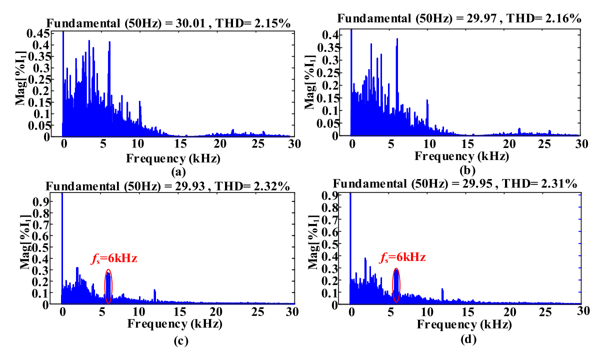

Fig. 14 Current spectrum. **a** Classic MPC. **b** WMPC. **c** M^2PC. **d** DSVM-OSS-MPC

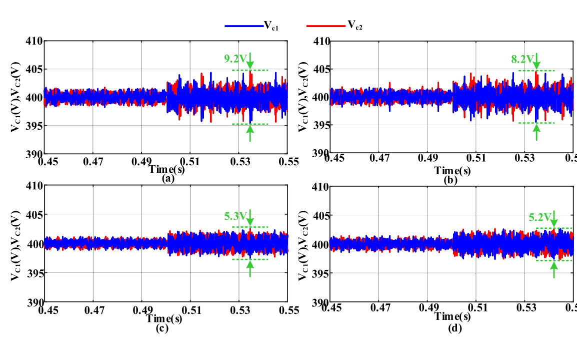

Fig. 12 Comparative evaluation of the NP voltage. **a** Classic MPC. **b** WMPC. **c** M^2PC. **d** DSVM-OSS-MPC

5.2 Experimental results and validation

The simplified diagram and a picture of the experimental set-up are presented in Fig. 15. The converter parameters and the grid voltage are given in Table 6. The different control algorithms are implemented in a real-time platform and further details can be found in [34].

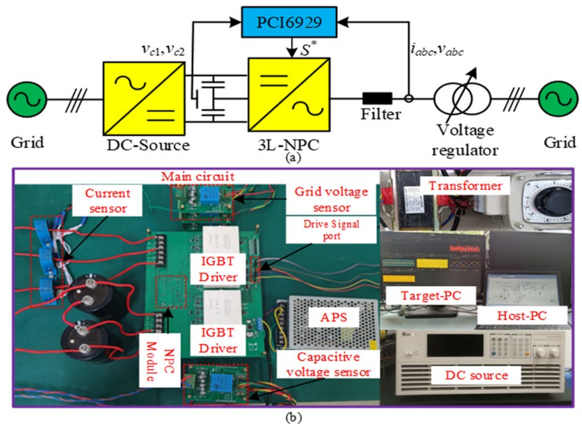

Fig. 15 Experimental system structure diagram. **a** Simplified diagram. **b**. Experimental set-up photograph

The comparative evaluation of the four control strategies at the same sampling frequency ($fs = 10$ kHz) is shown in Fig. 16, where the ASF of the classic MPC, WMPC, M^2PC and DSVM-OSS-MPC are 1.712 kHz, 1.704 kHz, 4.330 kHz, and 3.815 kHz, respectively. The operating average switching frequencies with M^2PC and the proposed method are over twice those with the classic MPC and WMPC. These results show that the current THD with MPC, WMPC, M^2PC and DSVM-OSS-MPC are $THD_{(a)} = 4.40\%$, $THD_{(b)} = 4.46\%$, $THD_{(c)} = 1.53\%$, and $THD_{(d)} = 1.57\%$, respectively. Compared with classic MPC and WMPC, the proposed control strategy provides a lower current THD. With the classic MPC and WMPC, the converter operates at a variable switching frequency with the average value lower than 5 kHz while both M^2PC and DSVM-OSS-MPC are operating at a fixed switching frequency of 10 kHz.

The comparative evaluation of the four control strategies at a similar average switching frequency (ASF = 3 kHz) is shown in Fig. 17, where the operating sampling frequency of the classic MPC, WMPC, M^2PC, and DSVM-OSS-MPC are 18 kHz, 18 kHz, 7 kHz, and 8 kHz, respectively. The four control strategies show similar current THD, i.e., $THD_{(a)} = 2.43\%$, $THD_{(b)} = 2.50\%$, $THD_{(c)} = 2.76\%$, and $THD_{(d)} = 2.71\%$, respectively. With MPC and WMPC, the converter operates at a variable

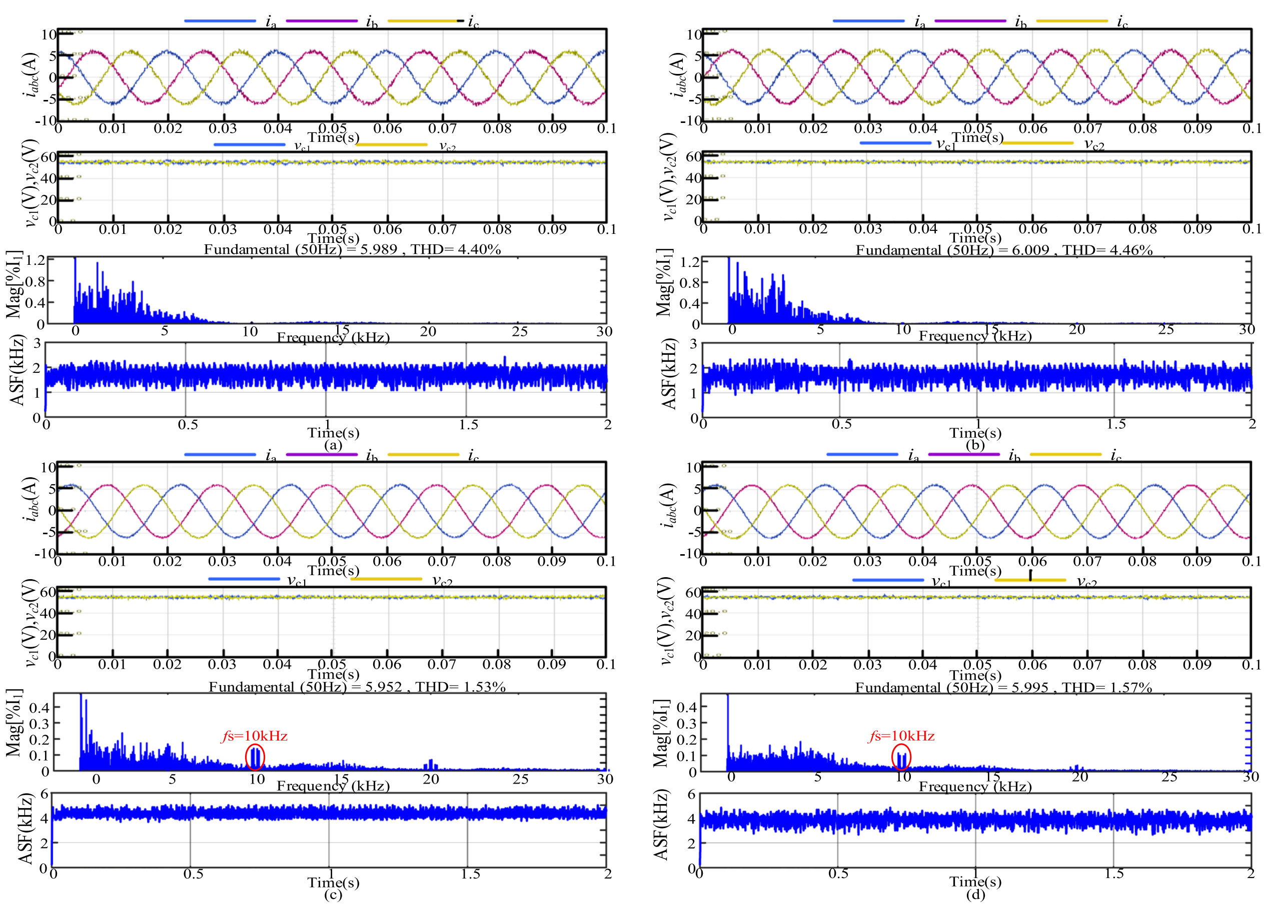

Fig. 16 Output current, capacitor voltage, current spectrum, average switching frequency, with ASF 1.712 kHz, 1.704 kHz, 4.330 kHz, and 3.815 kHz respectively. **a** Classic MPC. **b** WMPC. **c** M^2PC. **d** DSVM-OSS-MPC

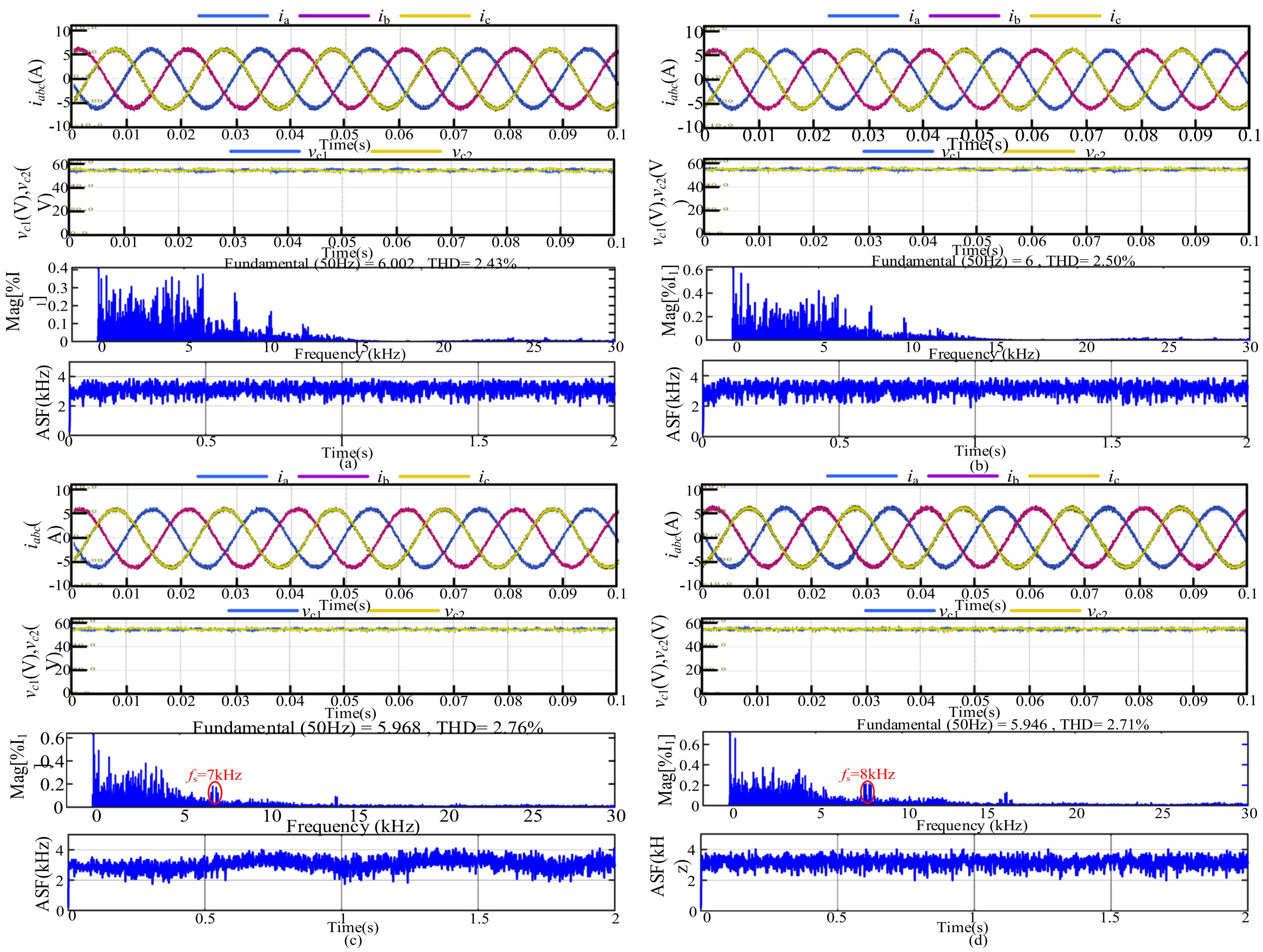

Fig. 17 Output current, capacitor voltage, current spectrum, average switching frequency with ASF 3 kHZ. **a** Classic MPC. **b** WMPC. **c** M^2PC. **d** DSVM-OSS-MPC

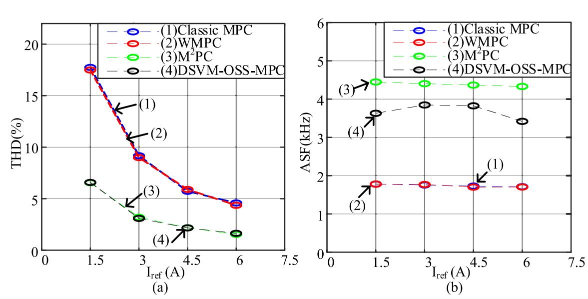

Fig. 18 The experimental results at the same operating sampling frequency. **a** current THD with the four control methods, **b** ASF with the four control methods

switching frequency while M^2PC and DSVM-OSS-MPC operate at a fixed switching frequency of 7 kHz and 8 kHz, respectively. To achieve a similar current THD as with M^2PC or DSVM-OSS-MPC, the sampling frequency of MPC and WMPC has to be increased, which is challenging to implement in low-cost digital processors.

The above results are further summarized in Fig. 18. The proposed controller results in a low current THD similar to the value under M^2PC. However, the operating average switching frequencies with M^2PC and the proposed method are almost twice those with the classic MPC and WMPC. When the resulting switching frequency is approximately the same with the four controllers as shown in Fig. 19, the proposed approach operating at 8 kHz sampling frequency results in slightly higher current THD than the values with MPC and WMPC since those are operating at 18 kHz sampling frequency. However, implementing MPC and WMPC at such a high sampling frequency can be challenging because of the computational requirement. Therefore, the proposed DSVM-OSS-MPC which has the lowest computation time is a suitable solution to improve

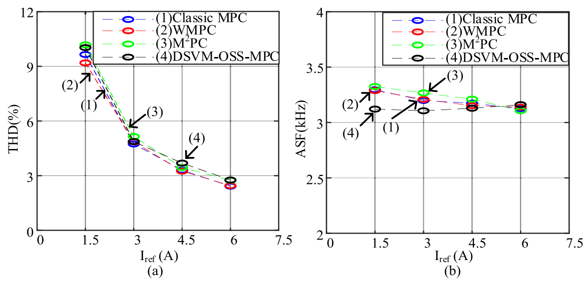

Fig. 19 The experimental results at around the same average switching frequency. **a** current THD with the four control methods, and **b** ASF with the four control methods

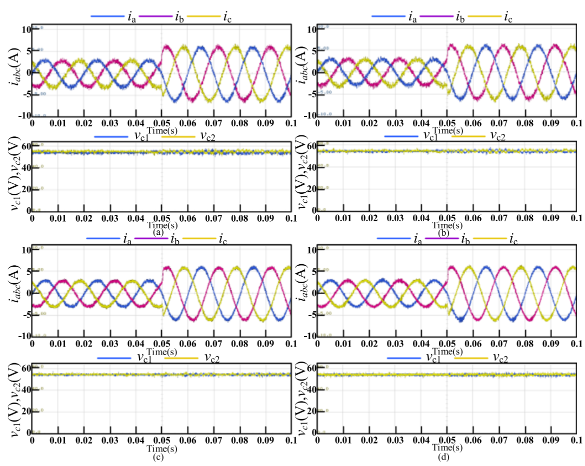

Fig. 20 Output current, capacitor voltage. (a) Classic MPC. **a** Classic MPC. **b** WMPC. **c** M^{2}PC. **d** DSVM-OSS-MPC

closed-loop performance in a scenario where a low-cost digital processor is used.

The dynamic responses of the current and capacitor voltages are shown in Fig. 20. As seen, the DC bus voltages remain balanced when the reference current is changed from 3 to 6 A. Compared with the classic MPC and WMPC, M^{2}PC and the proposed control strategy have faster response time.

To extract the computation times of the four control methods, each control algorithm is implemented in the TMS320F28379 DSP, and the digital output is set to a high voltage level when the algorithm is running and reset to a low voltage level when the processing is completed. The computation time required by each controller is presented in Fig. 21. As can be seen, the proposed strategy requires the lowest computational time of 23.26 µs, compared to 53.62 µs for M^{2}PC, which provides almost the same closed-loop performance for the same operating switching frequency.

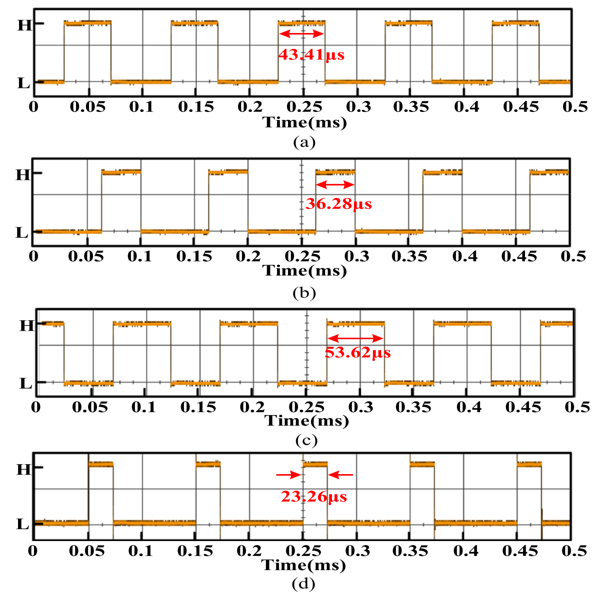

Fig. 21 Evaluation of the Computational Burden. **a** Classic MPC. **b** WMPC. **c** M^{2}PC. **d** DSVM-OSS-MPC

Table 7 Experimental and simulation comparison of the four methods

Method	Classic MPC	WMPC	M^{2}PC	DSVM-OSS-MPC
Weight coefficient	With	Without	Without	Without
THD	4.40%	4.46%	1.53%	1.57%
ASF	1.71 kHz	1.70 kHz	4.33 kHz	3.82 kHz
Frequency spectrum characteristics	Wide	Wide	Concentrate at f_s	Concentrate at f_s
V_o	$<1\%V_{dc}$	$<1\%V_{dc}$	$<1\%V_{dc}$	$<1\%V_{dc}$
Calculating time	43.41 µs	36.28 µs	53.62 µs	23.26 µs

The comparative study of the four control methods is summarized in Table 7. Compared with the classic MPC and WMPC, the proposed method significantly improves the accuracy of the current tracking, and the current harmonics are mainly concentrated on the fixed frequency. Compared to the M^{2}PC method, the proposed control strategy achieves similar control accuracy and THD performance. It's worth highlighting that the computation time of the proposed strategy is significantly shorter than the other methods, leading to a substantial reduction in computational burden. In addition, the proposed strategy limits the capacitor voltage imbalance to be less than 1%.

6 Conclusion

In this paper, a DSVM-OSS-MPC strategy operating with a fixed switching frequency is investigated for the control of a 3L-NPC inverter. The strategy is based on a cascaded MPC approach for controlling the grid current and balancing the capacitor voltages without any WF. To improve control precision, an optimal voltage is selected from the basic and virtual vectors of the proposed extended space vector method. In the proposed algorithm, the outer MPC employs an extended deadbeat method to output the optimal control voltage, reducing the execution time of the proposed control algorithm. The inner MPC evaluates the optimal vector and its potential redundancy, and selects the vector that minimizes the NP voltage. Additionally, each virtual vector is creatively synthesized as an OSS by using the DSVM and considering its impact on the NP voltage and the inverter switching commutations. The simulation and experimental results indicate that compared to the classic MPC and WMPC control algorithms, the closed-loop performance of the proposed algorithm is improved, and the current THD is maintained below 2%. The computational burden of the proposed strategy is reduced by over 50% compared to M^2PC with similar closed-loop performance, making it the most efficient option among all the compared methods.

It is evident that the proposed strategy offers the benefits of precise current response, capacitor voltage balance, absence of WF influence, and low computational burden. These characteristics render it suitable for application in 3L-NPC inverters. In future work, we will further explore and optimize this strategy in practical engineering applications while researching potential extension and enhancement to address the evolving challenges in grid-connected renewable energy generation.

Abbreviations

3L-NPC	Three-level neutral-point-clamped inverter
MPC	Model predictive control
VV	Virtual vectors
DSVM	Discrete space vector modulation
SS	Switching sequence
NP	Neutral point
THD	Total harmonic distortion
M^2PC	Modulated MPC
OSS	Optimal switching sequence
FCS-MPC	Finite control-set model predictive control
WF	Weighting factor
DSVM-OSS-MPC	Discrete space vector modulation and optimized switching sequence model predictive controller
ASF	Average switching frequency
WMPC	The FS-MPC without WF

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Author contributions
All authors contributed to the study conception and commented on previous versions of the manuscript. Sheng Zhou is the main contributor of the revised paper and completed the design, simulation, data analysis, and validation of the proposed method in the revised paper. Minlong Zhu completed the design and simulation of train working conditions in the origin submitted paper. Jiaqi Lin helped the hardware experiments, data collection, and modifying of the revised paper. Paul Gistain Ipoum-Ngome was mainly responsible for the selection of circuit parameters in the hardware design and put forward modification suggestions for the language of the paper. Daniel Legrand Mon-Nzongo guided the direction of the paper and put forward modification suggestions. Prof. Tao Jin proposed the idea and designed the methodology of this paper, and guided the direction of the paper. All authors read and approved the final manuscript.

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Availability of data and materials
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Declarations

Competing interests
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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